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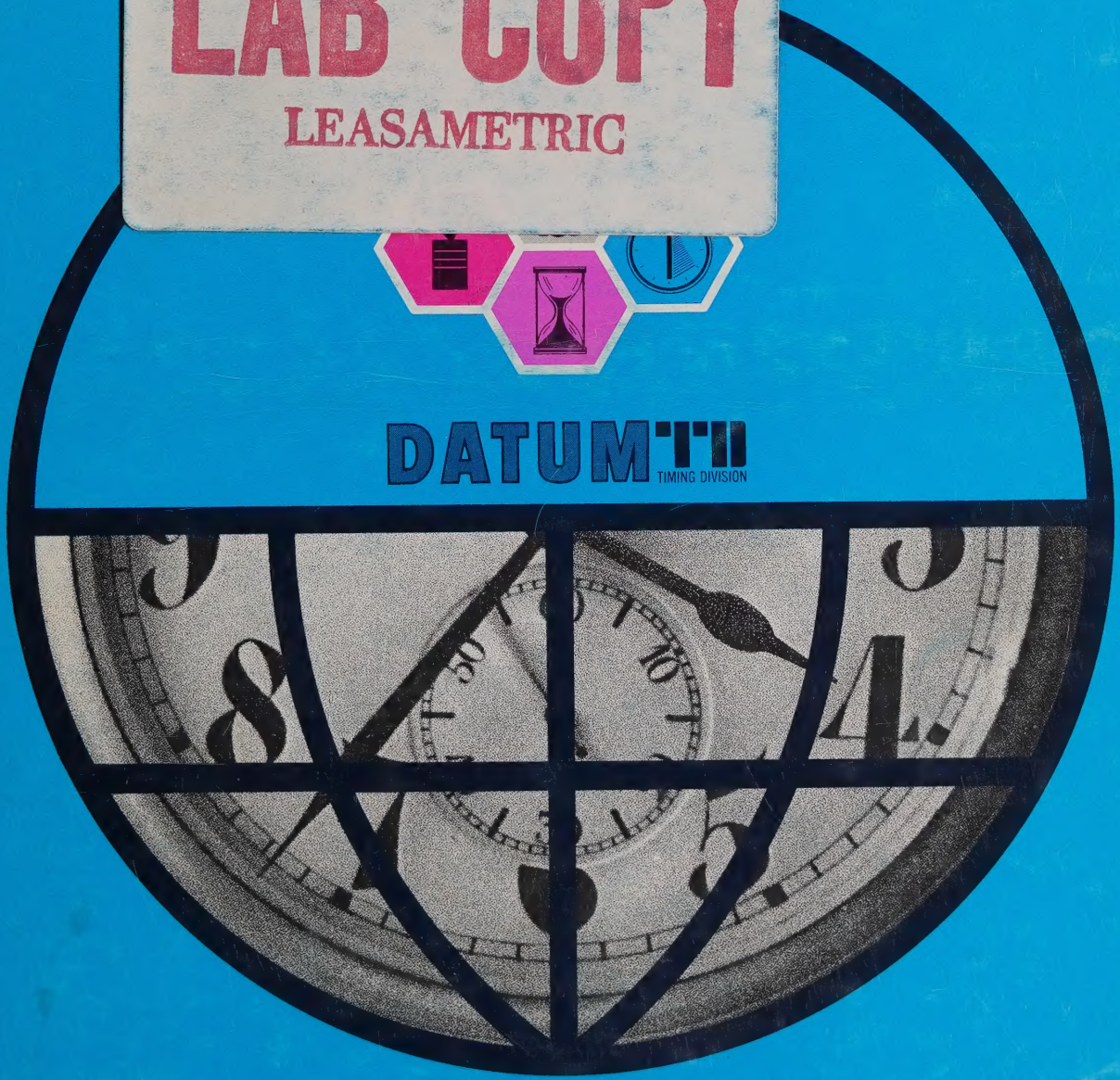
DATUM TTI
TIMING DIVISION



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ADDENDUM

In addition to the basic 9300 Time Code Generator/Translator, the 9300-708 contains the following option:

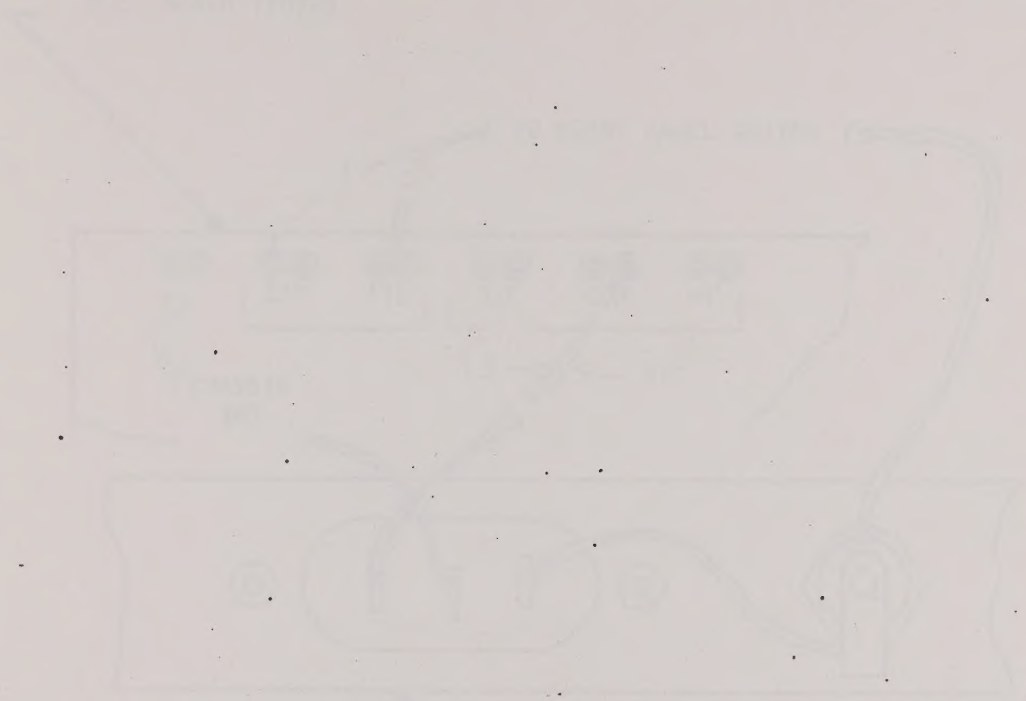
1. PARALLEL OUTPUTS
    a. See Drawing Number 16635 for logic.
    b. See Section II for specifications.
    c. Connector J4 (ms, S-M-H-D)
    d. See Table I for pin assignments.

TABLE 1

PIN ASSIGNMENTS

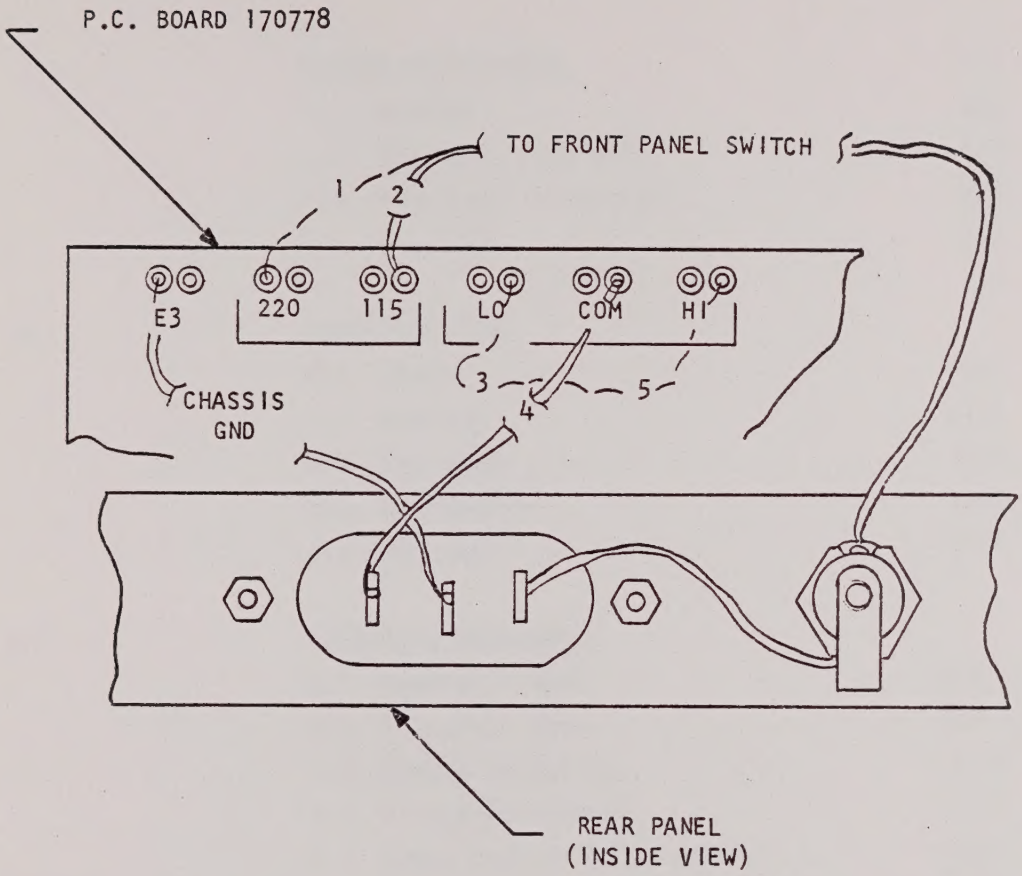
J4 Parallel Outputs (Binary Coded Decimal)

Pin	Term	Pin	Term
1	mS1	26	M40
2	mS2	27	H1
3	mS4	28	H2
4	mS8	29	H4
5	mS10	30	H8
6	mS20	31	H10
7	mS40	32	H20
8	mS80	33	D1
9	mS100	34	D2
10	mS200	35	D4
11	mS400	36	D8
12	mS800	37	D10
13	S1	38	D20
14	S2	39	D40
15	S4	40	D80
16	S8	41	D100
17	S10	42	D200
18	S20	43	D400
19	S40	44	D800
20	M1	45	FWD*
21	M2	46	FRP
22	M4	47	GO
23	M8	48	SAMPLE TIME
24	M10	49	$\overline{\text{SEARCH}}$
25	M20	50	GROUND



NOTE:

1. The Model 9300 is shipped for use with 115V AC operation unless identified for 220/230 VAC at AC power connector. See next page for changes to 220 VAC operation.



1. Jumper #1 For 220 VAC Operation
2. Jumper #2 For 115 VAC Operation
3. Jumper #3 For Lo Line Voltage
4. Jumper #4 For Normal Line Voltage
5. Jumper #5 For Hi Line Voltage

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SECTION I

SYSTEM DESCRIPTION

1.1 The Model 9300 Time Code Generator/Translator is designed to perform two basic functions. First, the unit generates a time code in suitable form for recording on magnetic tapes or paper charts. Secondly, the unit is capable of reading the recorded time when played back from a magnetic tape or other sources. The standard format includes BCD seconds, minutes, hours and days only in both the generator and translator modes.

1.2 TIME CODE GENERATOR

As a Time Code Generator the Model 9300 develops a serial, coded time code, modulated to allow recording on magnetic tape or to allow convenient distribution to remote users. The IRIG Format B is used so that the unit is compatible with many other existing facilities or other standard instrumentation equipment. The standard format is modified to include BCD seconds, minutes, hours and days only. Front panel controls allow the clock to be stopped, started or preset. Each digit of seconds, minutes, hours and days is settable to allow time-of-day or elapsed time operation. The basic clock accumulates time on a 24-hour basis and is accurately updated each second.

1.3 TIME CODE TRANSLATOR

When placed in the translate mode the unit will accept the standard IRIG B format either as generated in the Time Code Generator mode or as received from other sources. By using the standard IRIG Format B, the translator is usable in conjunction with other systems or projects. The unit automatically decodes the serial input code and provides a front panel display, serial pulse trains and optional digital outputs. Reading accuracy is better than 50 microseconds when reading in the forward playback mode.

A synchronization mode, selectable from the front panel, provides noise rejection. This feature allows the selection of "zero," "one," "two," "four," "eight," or "infinite" time frames bypass if input errors are detected. This feature is most important when digital outputs are required,

or tape search operation is desired. With "zero" selected each time frame is read. With one, two, four or eight selected, the unit is resynchronized only after the selected number of consecutive errored frames. With "infinite" selected, the unit updates from the carrier only and disregards the coded information. The unit must be synchronized in one of the other bypass positions prior to selecting the "infinite" mode.

1.4 PHYSICAL

The Model 9300 is constructed in a 1-3/4" package, requiring minimum 19" rack mounting or offering easy handling for desk mounting. A decimal display located on the front panel, shows either generated time or translated time depending on mode of operation. All operating mode controls are mounted on the front panel. Each display digit is individually presettable with a single thumbwheel switch and a pushbutton for each digit.

The circuitry of the Model 9300 consists of TTL and DTL type integrated circuits. Each element is mounted in a modular socket for ease in maintainability.

SECTION II

SPECIFICATIONS

2.1 INPUTS

2.1.1 J6 Power

a. 115/230 VAC ±10%

b. 48 to 420 Hz

2.1.2 J1 Code Input

a.	Format:	IRIG B BCD Time of Year (B122). (Control functions and straight binary seconds may be included in the code but are not recognized as valid data in the standard instrument.)
b.	Modulation Frequency:	1 kHz
c.	Modulation Ratio:	2:1 - 6:1
d.	Amplitude:	100 MV p-p to 10V p-p on the mark pulse.
e.	Input Z:	100 K ohm minimum
f.	Frequency Range:	10 Hz - 300 kHz
g.	Synchronization Accuracy:	Less than ±50 microseconds

2.2 OUTPUTS

2.2.1 J2 IRIG B: BCD Time of Year (B122)

(NOTE: This output is only available when operating in the GEN mode.)

a.	Carrier Frequency:	1 kHz sinewave
b.	Amplitude:	Adjustable from 0 to 10V p-p on the mark pulse.
c.	Modulation Ratio:	Adjustable from 2:1 through 4:1
d.	External Load:	$\geq$ 600 ohms

2.2.2 J3 Standard Pulse Rates

a. Rates:

1K pps	Pin 1
100 pps	Pin 2
10 pps	Pin 3
1 pps	Pin 4
GND	Pin 6

b. Duty Cycle: 80/20%

c. 1K pps: 50/50% (In translator mode)

d. On Time Edge: Negative

e. Output Levels: Logic "0" $\leq$ 0.4 VDC
Logic "1" $\geq$ 2.4 VDC

f. Source Impedance: DTL/TTL Compatible

2.2.3 Parallel Outputs (Optional)

a. (J4) 44 bit BCD time of year (millisecond, S, M, H, D)

b. (J5) 32 bit time of year (S, M, H, D)

c. Output Levels: Logic "0" $\leq$ 0.4 VDC
Logic "1" $\geq$ 2.4 VDC

d. Source Impedance: DTL/TTL Compatible

e. Sample Time: Approximately 1.5 μsec pulse to a logic "0" at update time (data is changing during pulse time). Sample time rate is normally 1 pps or 1 kpps (seconds or milliseconds output resolution).

2.2.4 J3 - Bi-Level Five Rate Slow Code (Optional)

a. Format: DATUM Slow Code

b. Amplitude: Adjustable - 10V (maximum) on the "mark" pulse.

c. Source Impedance: 100 ohms

d. Pin 5 - CODE
Pin 6 - GND

2.3 TIME BASE

a.	Type:	Crystal Controlled Oscillator
b.	Frequency:	1 MHz
c.	Stability:	$\pm 5 \times 10^{-6}$

2.4 ENVIRONMENT

a.	Temperature:	0°C to +50°C
b.	Humidity:	Up to 95% relative

2.5 PHYSICAL

a.	Panel Height:	1-3/4 inches
b.	Chassis Width:	17 inches
c.	Chassis Depth:	18 inches

SECTION III

OPERATING PROCEDURE

3.1 GENERATE MODE

a. Apply 115V AC power to J6

b. Turn on instrument by moving the PWR switch, located on the front panel, to the ON position.

c. Rotate the MODE switch to the HOLD position. (Display should be stationary.)

d. Preset the time of day using the following procedure:

   1. Start with the least significant digit (unit seconds) and in progression finish with hundreds of days.
   2. Select the number to be preset into each decade with the Preset thumbwheel switch.
   3. Press the pushbutton under each decade to enter the PRESET number into the output register.

e. Rotate the MODE switch to the GEN position. At the preset start time, press the START pushbutton.

f. The display will now update at a 1 pps rate and all outputs will be available on their respective output connectors.

3.2 TRANSLATE MODE

a. Apply power as in steps a and b of the GENERATE MODE procedure.

b. Place a standard 1 kHz modulated IRIG B code on BNC connector J1 located on the rear of the unit. It does not matter if the code format has been modified to remove the control functions or straight binary seconds as this portion of the time code is not used for decoding purposes in the 9300. (See 9300 specifications for modulation ratio, frequency range and amplitude requirements.)

c. Rotate the MODE switch to the TRANS position.

d. Place the FWD/REV switch to the FWD position.

e. After allowing approximately one minute after turn-on for the AGC to settle, the 9300 will autometically synchronize to the input time code.

3.3 BY-PASS OPERATION (See also paragraph 3.12)

a. Select TRANS. The 9300 will respond to each time frame of the input code. Any degradation of the input code may cause an erroneous reading on the 9300 Time Code Generator-Reader.

b. Select 4. The 9300 will sync to the input code, then automatically lock out its own sync circuits and just monitor the input code for time differences. Frame errors are counted; however, the 9300 synchronization is not disturbed unless four consecutive errored frames are counted. If frame errors are separated by a valid frame, the error counter is reset to zero; therefore, resynchronization can only take place on the fifth frame after counting four consecutive errored frames. This mode can be extremely useful when input time code is noisy or being derived from a poor or spliced tape.

c. oo BY-PASS. Note: Prior to selecting this position, the 9300 must be synchronized in either the TRANS, 1, 2, 4, or 8 position. After synchronization, rotate the MODE switch to the oo Bypass position. Once in this mode, all synchronizing functions are locked out and the 9300 will act as an elapsed time generator updating on the carrier rate of the input code.

3.4 DIRECTION CONTROL

The 9300 is provided with manual direction control and is operated by means of a front panel mounted toggle switch, INPUT FWD/REV. For forward operation place this switch in the FWD position. For reverse translation, place the switch in the REV direction.

3.5 INPUT CODE POLARITY CONTROL

The 9300 includes provisions to compensate for inverted polarity input codes. This is done with a front panel mounted toggle switch, INPUT +/-. For normal operation, this switch should be placed in the (+) position. For inverted polarity input codes, place the switch in the (-) position.

3.6 INTERNAL FILTER CONTROL

An internal 3 kHz low pass filter has been provided in the 9300, for use in playback (X1 speed ratio) operation. To activate the filter, place the front panel mounted FILTER IN/OUT switch to the IN position.

3.7 TAPE SEARCH OPERATION (Optional)

a. Connect the 9300 to the Tape Search unit as described in the Tape Search unit instruction manual.

b. Insure that the FWD/REV switch is in the FWD position and that the FILTER switch is in the IN position.

c. A logic "1" on Pin 45 of J4 will program the 9300 for forward operation, a logic "0", for reverse operation.

d. A logic "1" on Pin 49 of J4 will activate the low pass filter, a logic "0" will de-activate the filter.

e. A logic "0" Pin 47 of J4 will inhibit updating of the 9300.

3.8 5 RATE SLOW CODE (Optional)

The PRESET thumbwheel switch serves a dual function when the Slow Code option is installed. In addition to serving in the PRESET function, positions "1" through "5" select the desired frame period (see slow code drawing in Section V). Position "0" de-activates the Slow Code circuitry.

3.9 INPUT CODE SELECT (Optional)

Rotate the MODE A/B/E switch to program the 9300 to accept either IRIG A, IRIG B or IRIG E as the input code.

3.10 ADVANCE/RETARD (Optional)

a. Preset and start the generator as described in paragraph 3.1 above.

b. Sync an oscilloscope on the "on-time" edge of an external reference pulse (1 PPS).

c. Observe the "on-time" edge of the equivalent local pulse rate. If the local pulse appears to the right of the reference, the 9300 is "late." If the local pulse occurs to the left, the 9300 is "early."

d. Select the greatest Advance/Retard rate (refer to SWITCH & CONTROL LOGIC (11) drawing for rate identification) which will not overcorrect for the offset in one second. For example: for an offset of 5 milliseconds, the proper rate would be 1 millisecond/second, as 10 milliseconds/sec would overcorrect.

e. If the local pulse is "early," press the RET pushbutton. If the local pulse is "late," press the ADV pushbutton. Observe that the local pulse appears to move toward the reference pulse.

f. When the local pulse is within one second correction capability, select the next slowest correction rate.

g. Continue in this manner until the local pulse is alligned to within the maximum resolution of the Advance/Retard circuit.

3.11 EXTERNAL START (Optional)

a. Connect the external start pulse (1 PPS) to the INPUT BNC on the front panel. Place the WWV/DC switch in the appropriate position in accordance with the type signal to be used. Observe that the TICK indicator blinks at a 1 PPS rate.

b. If a WWV "tick" is being used, rotate the LEVEL control to the maximum counter-clockwise position. Adjust this potentiometer clockwise to obtain a steady blinking of the TICK indicator. Setting the control more clockwise than required to obtain a reliable indication may result in an unreliable start.

c. Preset the generator as described in steps 3.1. Rotate the MODE switch to the GEN position.

d. After the "Tick" which occurs one second prior to the preset start time, press the ARM pushbutton. The ARMED indicator will light.

e. The next "Tick Pulse" will start the generator.

3.12 DETAILED BY-PASS OPERATION

When this switch is set to "0" (TRANSLATE), the instrument monitors the input code and responds to each time frame of the input code. If the coded input is erroneous, the unit outputs the incorrect input value on both the visual display and the optional BCD output. However, the ERROR indicator is enabled (because a difference exists between the input and internal time values). This error status will remain until a subsequent code frame is input which is in agreement with the internal time value.

When this switch is set to "4", the instrument monitors the input code and if one or more frames are in error (up to 4), continues to properly update the displayed and BCD outputs by utilizing the 1 kHz carrier of the time code. Two (2) conditions affecting the ERROR indicator are as follows:

a. Less than four (4) consecutive 'erroneous' frames. The ERROR indicator is energized as long as a difference in time value exists between the input code and the internal time registers. At the end of a frame received in agreement with the internal time value, the ERROR indicator is de-energized.

b. Four (4) or more consecutive 'erroneous' frames.

   The ERROR indicator is energized as long as a difference in time value exists between the input code and the internal time registers. During the fifth consecutive frame, the time value

of the input code is entered into the internal time register. If the sixth consecutive frame of the input agrees with the updated time value in the internal time register, the ERROR indicator is de-energized at the end of this frame. However, if the sixth frame of the input code does NOT agree with the updated time value in the internal register, the input code value is again entered into the internal register and the next frame is again examined for agreement with the 'new' time value. The ERROR indicator remains energized and each subsequent frame time value is entered until time value agreement is found.

When the switch is set to "∞" (infinity), the instrument acts simply as an elapsed time generator, updated from its last time value by the carrier input. The ERROR indicator is energized when a difference in time value exists between the input time code and the internal time register and is de-energized at the end of the first frame found to be in agreement. Entering of input code time value(s) is inhibited whenever the switch is in the "∞" position.

Thus, the ERROR indicator is energized whenever (irrespective of switch position) a time value difference is detected between the code and the internal time register. Further, this status is de-energized at the end of the first subsequent code frame time value found in agreement with the internal time register. Therefore, the effect of the switch positions is to allow entering (jamming) of the input time code value into the internal time register under the following conditions:

a. "0" - each frame
b. "1" - the frame following a detected 'errored' frame
c. "2" - the frame following two (2) consecutive detected 'errored' frames
d. "4" - the frame following four (4) consecutive detected 'errored' frames
e. "8" - the frame following eight (8) consecutive detected 'errored' frames
f. "∞" - never

Finally, from the above examples, it may be discerned that the 'meaning' of the energized state of the ERROR indicator is that a difference in time value exists between the input code time value and the internal register time value and that the de-energized state of this status means there is no detected difference in these values.

SECTION IV
ADJUSTMENTS

The following is a list of adjustments which are basic to the 9300 Time Code Generator/Reader and includes those assemblies which are basic options. In the case of "Potentiometers," they are set at the factory to a nominal setting as indicated in ( ). However, the user should refer to the top assembly drawing for the location of these variables and adjust them for users specific requirements.

1. SINEWAVE SHAPER/MODULATOR ASSEMBLY
   a. R17 Level Adjustment. Range 0 to 10V peak to peak on the mark amplitude of the output code (3V p-p).

   b. R15 Modulation Ratio Adjustment. Range 2:1 - 4:1 mark to space ratio on the output code (3:1).

   c. R7 Phase Adjustment. Sets the phase of the carrier frequency so there is no discontinuity when amplitude modulation takes place.

2. POWER SUPPLY ASSEMBLY
   a. R10 adjusts the output level of the +5 volt regulator. Should be set to +5V ±2%.

3. SLOW CODE ASSEMBLY (Optional)
   a. R12 adjusts the output level (+6V mark amplitude)

SECTION V

THEORY OF OPERATION

5.1 LOGIC DESCRIPTION AND USE

The 9300 is depicted by several drawings. One of these is the top assembly drawing which shows the physical location of the assemblies that are contained within the instrument. This print should be used to locate connectors on the rear panel and for quick reference to the physical location of any of the assemblies or controls.

In the title block of each logic print is a circled number. For instance, the IRIG basic print (Minor Time) has circled number (8) in the title block. The IRIG basic print (Major Time) has circled number (9). The LED display has circled (12) in the title block. Except for terms originating within the drawing being studied, this reference number will precede each term, showing the sheet of logic upon which it originated. To use these numbers. simply observe the term, look at the term reference number in front of the term, then select the print that has this reference number in the title block. This print will show the point of origin of the term you are trying to find. This provides a convenient means of getting back and forth from various pages of these logics.

Each time a term reference number will refer you back to the source of that signal. In each of the logics there will be a number such as A4, A8, A11, etc. These number refer to the physical location on this assembly for that particular integrated-circuit element. In order to determine a physical location of an integrated circuit, one would merely refer to the top assembly drawing. In the lower left-hand corner of this drawing, each assembly contained within the instrument is listed, prefixed with a code letter, (Ⓐ Ⓑ Ⓒ etc.) then, by referencing the mechanical view of the top of the instrument, look for the board labeled with that code letter. Examine the board until the desired integrated circuit is located.

All references in this discussion will be based on the circled term reference numbers located in the title blocks of all logic prints. The reader should be familiar with the above before preceeding.

5.2 GENERAL

The Model 9300 is both a time generator and a time translator. A time generator is a device which takes a referenced frequency and divides it so as to accumulate or "count" time intervals. A time translator is a device which requires a serial coded input and "decodes," or "translates" this input to some other form, usually parallel time data.

In order to better understand the logic organization of the 9300, let's first review the basic configuration of typical timing units.

Figure 5-1 shows a simplified diagram of a typical Time Code Generator. The significant sections of a Time Code Generator are:

a. Frequency Source - Usually a crystal-controlled oscillator.

b. Minor Time Counters - The purpose of these counters is to develop scan terms and rates required to develop the serial code format or to be used for parallel outputs. They also supply a 1-pps signal that is used to update the Major Time Accumulator.

c. Major Time Accumulator - This section is a counter whose function is to store the time-of-year data. It is incremented by the 1 pps clock output of the frequency dividers. Its outputs are buffered and used for parallel outputs or they are scanned by the encoder and outputted in a serial format.

d. Counter Control - This section synchronizes the time accumulator and includes switches to select and enter the time-of-day into the Major Time Accumulator.

e. Parallel-to-Serial Converter - This section consists of scan gates that serialize the contents of the accumulator into a continous pulse train.

TYPICAL TIME CODE GENERATOR

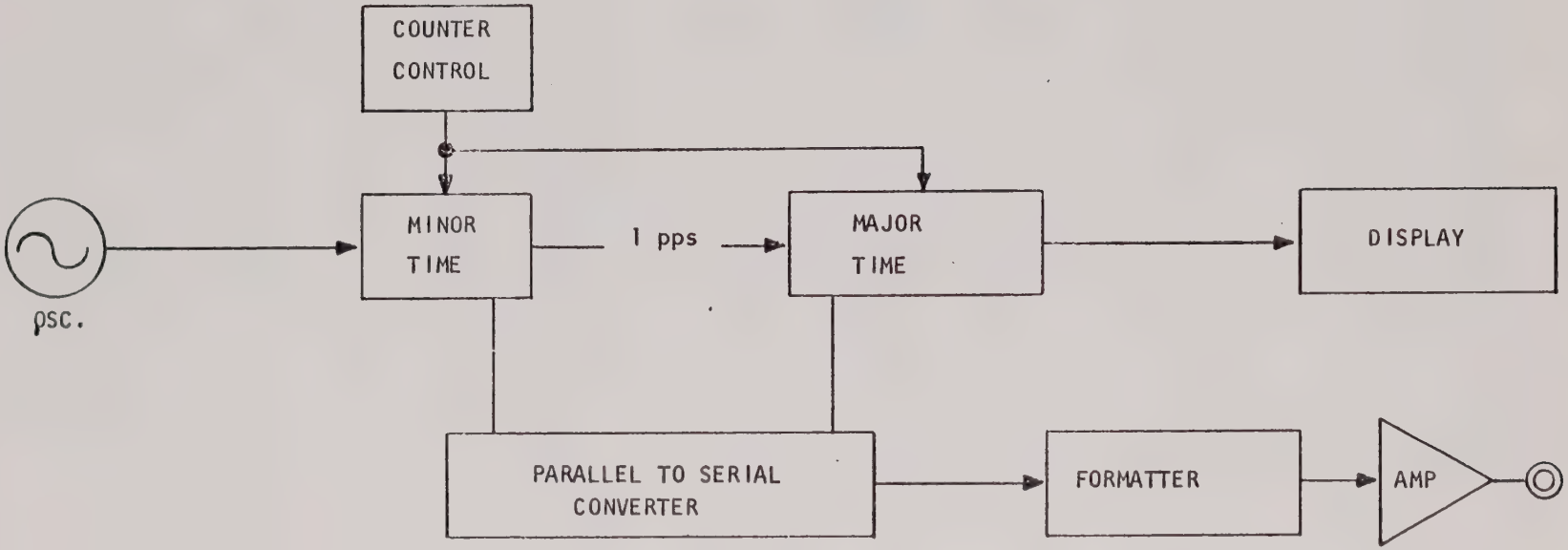


FIGURE 5-1

f. Formatter - This section uses pulse rates from the minor time counter to obtain the pulse widths and index pulses required to provide the format defined by the type of time code being generated. This format is then usually combined with a sinewave to provide an amplitude-modulated signal.

g. Output Amplifier - This section provides the required output drive and signal levels of the formatter output.

h. Display - This section interfaces the generator with the operator.

Figure 5-2 shows a simplified diagram of a typical Time Code Translator. The significant points to a Time Translator are:

a. Input Amplifier - Usually this is an AGC type amplifier. Its function is to provide a constant amplitude signal to the decode and detection circuitry.

b. Serial to Parallel Converter - This is the heart of the unit. Its function is to detect digital data in the input format and assign it to storage in the time accumulator. This portion contains the necessary circuits to synchronize the frequency dividers.

c. Frequency Dividers - These counters divide the carrier frequency. Once synchronized by the decoding circuitry in the serial-to-parallel section, this counter provides the terms necessary to index the digital data contained in the input code. This allows the locating of each code bit and the proper assignment to accumulator storage. Also important, they provide a 1 pps signal to update the Time Accumulator.

d. Time Accumulator - This counter stores the value being read from the input code. It is updated with the 1 pps signal from the frequency dividers and is permuted to count in the format of the input time code (usually seconds, minutes, and hours). Day-of-year may sometimes be provided if required

TYPICAL TIME CODE TRANSLATOR

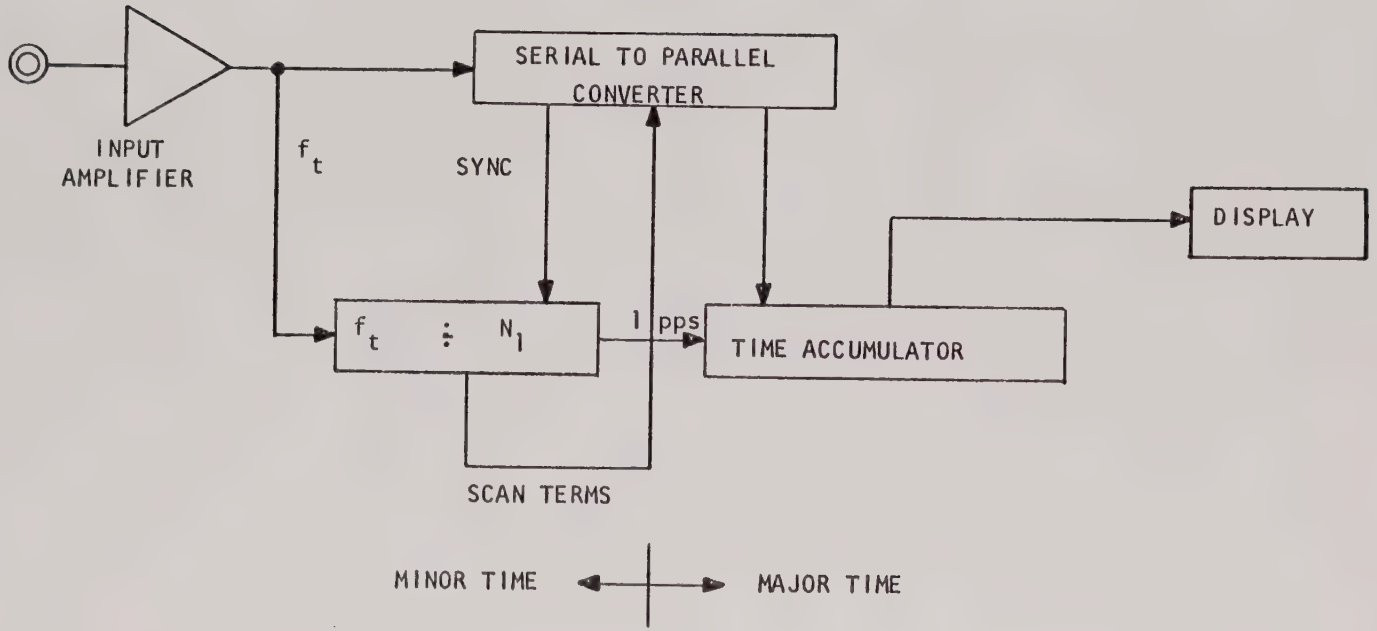


FIGURE 5-2

and it is contained in the input time code. The Time Accumulator is the basis for most outputs required by the unit.

e. Display - This section takes the Time Accumulator data and displays it for the user.

Now if we combine the two functions, taking advantage of circuitry found common to both, we obtain a Time Code Generator/Translator (Figure 5-3). Logic functions which are common, i.e., those which need not be duplicated are:

a. Frequency dividers (all of those in the translator and at least half of those in the generator).
b. Time Accumulator
c. Display

Of course, the power supply and chassis are shared.

5.3 DETAILED LOGIC DESCRIPTION

This description will be referenced only to the term reference numbers that are contained within the title block of each individual logic print. Before proceeding, the reader should be familiar with paragraph 5.1, LOGIC DESCRIPTION AND USE.

(1) AGC

The automatic gain control amplifier assembly contains the input amplifier and the code strippers required to normalize the input and derive the necessary clock signals for the decoder.

The AGC amplifier is wideband so as to make the unit operational where variations of input signal frequency as well as amplitude is experienced such as in tape search applications.

Generally if a translator is used as a single purpose unit such as to only translate code at a single rate and display it, the AGC circuits can be narrowband. To make the unit more adaptable to different types of applications, we have provided a 100 MV to 10 volt dynamic range and a frequency response of 25 Hz to 300 kHz. The circuit does not require adjustment over this range.

TYPICAL TIME CODE GENERATOR/TRANSLATOR

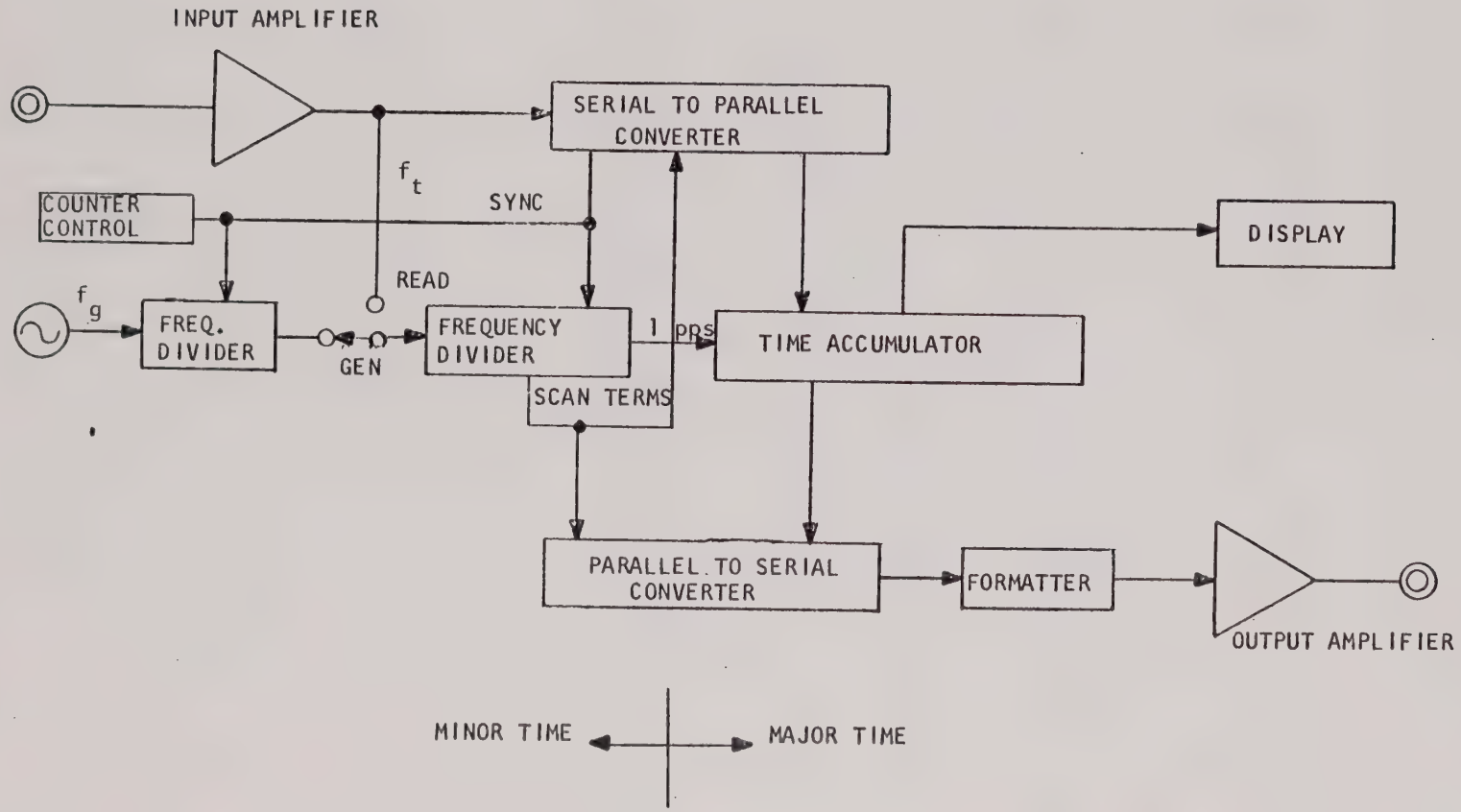


FIGURE 5-3

After the input signal is normalized by the AGC, preset level comparators develop clock signals used for decoding. ØA which occurs at the positive zero axis crossing of the carrier, is used throughout the unit for clocking and synchronization. ØC is the mark clock which occurs only each half cycle of the carrier modulation (mark amplitude cycles).

Figure 5-4 shows a typical modulated signal. Two cycles are modulated. Examples of ØA and ØC are shown relative to the signal. Observe also the other definitions provided.

(2) DECODER

This logic uses the terms ØA, ØB and ØC from the AGC (1) to reconstruct the D.C. envelope of the input code. The logic symbol identified as DF3 represents this reconstructed envelope.

A binary counter is used to count the number of "mark" cycles that are contained during each positive excursion of DF3. Whenever four or more "mark" cycles are counted, the term BIN1 (Binary 1) will go to a logic "one" indicating the presence of a Binary One in the code. When eight "mark" cycles have been counted, the term PIC (Position Identifier Count) will go to a logic "one". The coincidence of PIC with DF3 being clocked off causes the logic term identified as PID (Position Identifier Detector) to go to a logic "one" indicating the detection of one of the ten position identifiers contained within the IRIG format.

Once per frame, the terms PIC, PID and DF2 coincide. This occurs at plus nine milliseconds in IRIG B and the decoded combination is used to fire the frame sync one-shot (FS). This pulse is used to sync the minor time counter (8) to a count of nine. Thus causing the minor time counter to be synchronized with the input time code.

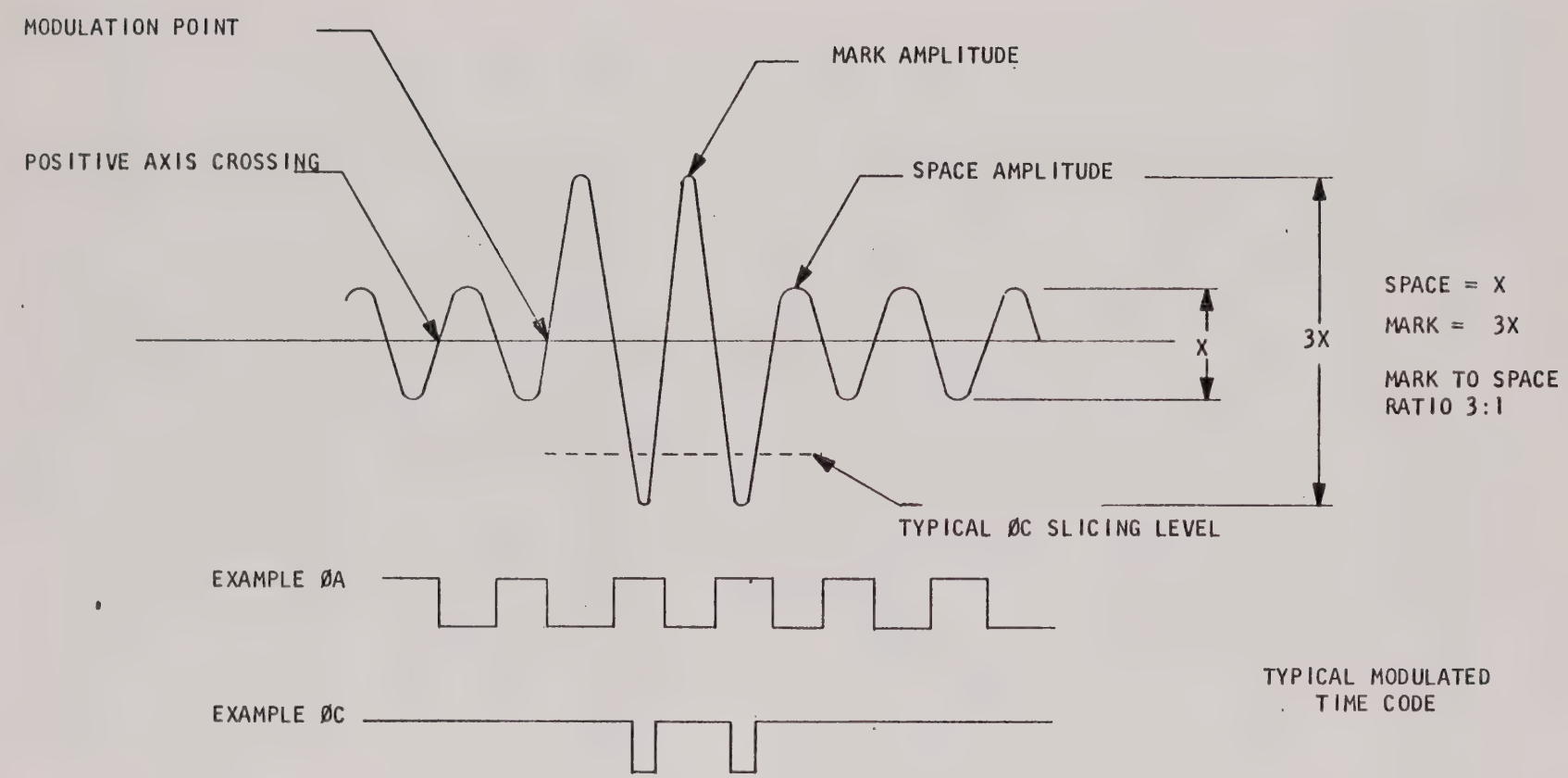

MODULATION POINT
MARK AMPLITUDE
POSITIVE AXIS CROSSING
SPACE AMPLITUDE
X
3X
SPACE = X
MARK = 3X
MARK TO SPACE RATIO 3:1
TYPICAL ØC SLICING LEVEL
EXAMPLE ØA
EXAMPLE ØC
TYPICAL MODULATED TIME CODE

FIGURE 5-4

(3) MODE CONTROL

This logic contains the steering logic necessary to program the unit for the generate or translate mode of operation and to condition the unit for forward or reverse translation and to accept normal or inverted polarity input code.

In the generate mode, the unit is programmed for forward operation. In the translate mode, forward or reverse translation is controlled by the FWD/REV switch on the front panel or via the rear panel (FWD*) if the optional parallel outputs are installed. A front panel switch conditions the unit to accept normal (+) or inverted (-) polarity input codes.

This logic also contains a four-bit serial-to-parallel converter which converts the serial time information (BIN1) from (2) and converts this data to four lines of parallel data (SF1, 2, 4, or 8) in the translate mode. In the generate mode, the contents of the PRESET thumbhweel switch are passed directly through. These outputs are bussed common to the "D" inputs of the major time accumulators on (9). This allows for presetting the desired start time when in the HOLD mode or for loading the time content from the input code when in the translate mode.

Also contained on this logic is a two-way, four-bit data selector used to select the appropriate clocks for the serial-to-parallel converter (SFS) and the milliseconds counter (CMSC*) as well as two synchronization pulses ($\overline{FS}$* and $\overline{GFS}$*) in the generate or translate mode of operation. The serial-to-parallel converter is clocked by the 1 MHz clock (MCC) in the generate mode and by a decoded term from the Decoder (2) in the translate mode. The milliseconds counter is clocked by either tmSC8 in the generate mode or by ØA* in the translate mode.

Portions of four logic elements C3, D3, D9 and F9 are cross-gated to form the RUN/HOLD latch. In the generate mode, rotating the MODE switch to the HOLD position causes $\overline{\text{HOLD}}$ to become a logic "0", stoping and resetting the minor time counter (8) and enabling major time preset push-buttons via the term $\overline{\text{PSE}}$.

An "exclusive-or" element, D8 pins 1, 2, and 3 provides for a low-pass filter in the AGC to be activated by either the front panel FILTER IN/OUT switch (1FSC) or via the rear panel ($\overline{\text{SEARCH}}$) from the optional parallel outputs.

(4) SCAN LOGIC

This logic is used to generate the load pulses necessary for strobing the parallel data from the serial-to-parallel converter on (3) into the major time counter (9).

Assignment to the proper group (seconds, minutes, hours or days) is accomplished by logic elements C5 and C7. Assignment to the proper portion of each group is accomplished by logic elements E6 and E7 which generate units data strobe pulses (UDSF, UDSR) and tens data strobe pulses (TDSF, TDSR) for both forward and reverse operation.

Forward or reverse strobes are selected by logic element D7. The two load pulses are factored by the one-shot SPG which limits the strobe pulses ($\overline{\text{SPA}}$ and $\overline{\text{SPB}}$) to a duration of approximately one microsecond. $\overline{\text{SPG}}$ inhibits the strobes in the generate mode; or, in the translate mode, until the selected number of errored frames (EC8) from sync mode logic (5) are counted.

(5) SYNC MODE

This logic performs as a digital filter to prevent erroneous information from being displayed or from disturbing the various outputs.

The output of the IRIG Encoder ($\overline{DCSC}$) (32) is serially compared with the comparable decoder output ($\overline{DF2}$). IF a discrepancy exists between the two, the error detector flip-flop ECD clocks "on". When ECD is reset at the end of the frame, the error counter element C10 is clocked one time. The setting of the MODE BYPASS switch (1, 2, 4, 8, oo) determines how many errored frames will be counted before the counter output EC8 goes true. When this occurs, the error counter clocks are inhibited and the scan logic is enabled, allowing the input data to be loaded into the major time counter and allowing the minor time counter to be re-synchronized via the term $\overline{GFS}$.

If a valid frame (ECD not clocking on) occurs before reaching the selected number of errored frames (EC8 not clocking true), the error counter is reset via the term $\overline{REC}$. Therefore, the units synchronization will not be distrubed until the selected number of errored frames have been counted.

With the MODE/BYPASS switch in the TRANS position, EC8 is held true continuously, therefore the unit is synchronized each frame. With oo selected, the unit is never synchronized to the incoming code and acts as a generator, using the input code carrier as a time base.

The sync mode circuitry is disabled in the generate mode and when operating in the reverse direction.

(7) TIME BASE

This logic provides the 1 MHz time base for the generator. Four time bases are available: Two different 1 MHz crystal oscillators, a 10 MHz crystal oscillator and a divide-by-ten element, or an optional external 1 MHz sine-wave input with a level converter. The output is a TTL 1 MHz pulse (MCC).

(8) MINOR TIME

This logic consts of a series of decade counting units (DCU's) which accept the 1 MHz clock from (7) and divides it to 100 KPPS (μsc8), 10 KPPS (hmsc8), 1 KPPS (tmsc8), 100 PPS (msc8), 10 PPS (hsc8), and 1 PPS (tsc8). The term $\overline{HOLD}$ prevents the minor time counter from updating and holds each decade reset when in the HOLD mode. Also contained on this logic are four buffers which isolate the four standard pulse rate outputs.

(9) MAJOR TIME

This logic consists of a series of UP/DOWN counters which accept the 1 PPS clock (cUSC) from (8). This clock is divided down to one-pulse-per-minute at B9 pin 6, one-pulse-per-hour at B7 pin 6, one pulse-per-day at B5 pin 2 and one pulse-per-thousand days at B2 pin 7.

The tens-of-seconds counter, B9, is forced to recycle at the end of sixty seconds by one-shot RTS which "fires" at a decoded count of sixty (TSC4·TSC2). Similarly, the tens-of-minutes counter, B7, is reset at sixty minutes by RTM and the hours counters B5 and B6 at twenty-four hours by RHC.

Presetting the major time to the desired start time in the HOLD mode or to the contents of the input time code in the translate mode is accomplished by lowering the preset pin 11 of the selected decade to a logic "0". This is done via the pushbuttons beneath the associated digit of the display in the HOLD mode and via the strobe pulses from (4) in the translate mode. When this is done, the selected decade is preset to the state of the four preset lines, SF1, 2, 4, and 8.

(10) DISPLAY DRIVERS

This logic consists of a series of four-to-seven line decoders which converts the four-line BCD output of the major time counter (9) to the seven-line format required by the L.E.D. Display (12).

(11) SWITCH & CONTROL LOGIC

This print serves as an interface drawing used to indicate interconnections between the various assemblies within the unit as well as illustrating the various input and output connectors, with the exception of the parallel outputs which are described in a separate logic description.

(12) LED DISPLAY

This logic consists of nine seven-segment Light Emitting Diode (LED) display units. Each converts the seven-segment outputs from (10) to a visible display for interface to the user.

IRIG B Encoder (32)

Terms from the minor time counter are used to sequence multiplexer chips A9 through A14. The output of the major time counter is then scanned and grouped into ten bit serial words, X0 through X4. X0 contains the serial time information of units of seconds and tens of seconds. X1 contains the serial time information of units of minutes and tens of minutes. X2, units hours and tens of hours, X3 unit days and tens of days, and X4, hundreds of days. The terms X0 through X4, are again serially selected bit by bit by means of IC A15 and outputted as the term $\overline{D}$ on pin 6 of A15. $\overline{D}$ now represents the time of year information in a serial form.

Although the data at this point is serial, it is still not in an IRIG B format. The IRIG B format is generated by the output term DCSC and the collection of gates that control this reset line on pin 4 of A7. DCSC is enabled at a 100 pps rate and clocked true by the 1000 pps clock applied to pin 12 of A7. The reset occurs whenever the enable term of pin 4 a A7 is set to a "one" state. This occurs at 2 milliseconds if neither a position identifier is contained at that particular period or a binary "1" is not present in the code. However, if a binary "1" is present in the serial time information being generated at A15, pin 6, the reset of DCSC is delayed until the count of 5, or 5 milliseconds.

At a 10 pps rate, at a count of 9, the DCSC reset enable is delayed for 8 counts, thus generating an 8 millisecond wide position identifier. Once per second, at T-zero time, A7 pin 5 (X0Y0) is set true. This generates the frame reference pulse of the IRIG B time code and prevents the first pulse of each frame period from being reset until a count of 8 milliseconds. The output of DCSC is buffered and presented as the DC shift code output.

On (32A) the output of A8 pin 6 is a 1 KC squarewave. The odd harmonics are filtered from the squarewave to generate a sinewave is modulated by the DC code envelope ($\overline{DCSC}$) by means of FET Q1 and IC A17. The output of A17, pin 1, is attenuated by a potentiometer, R17, which is used to set the level of the IRIG B modulated serial time code. The output amplifier consists of A17, Q2 and Q3. The gain is set by resistors R18 and R20 and is set to be a fixed gain of 10. The modulated output is available on E6.

POWER SUPPLY (49)

The Power Supply furnishes regulated ±15V DC and +5V DC to the unit. The ±15V DC regulators are integrated circuit regulators with internal fault protection. The +5V DC regulator employs and LM305 voltage regulator and is of the switching type.

The LM305 is essentially an operational amplifier with a built-in Zener reference. When the voltage on pin 6 falls a few millivolts below that of the internal reference, Q1 and Q2 are turned on and the voltage on the 5-volt line begins to rise. Q1 and Q2 turn off as the voltage on A1-6 rises above the reference level. L1 tries to maintain constant current flow and current begins to flow through CR2. This continues until Q1 and Q2 are again turned on and the cycle is repeated.

The switching regulator is thus an efficient method of obtaining constant 5V DC from an unregulated source, since power is dissipated in Q1 only when it is on or changing states.

For 5 volts from a 23V source, Q1 is on approximately 25 percent of the time. Q3 and Q4 provide short circuit protection by forcing the regulator to decrease the output voltage when the current through R7 becomes excessive. When the output voltage becomes too high, CR5 conducts and CR6 is turned on. The current limit circuit then shuts down the regulator.

OPTIONS

Described in the following paragraphs are some (but not all) of the options and capabilities which are available. For instance, Control Functions and/or Binary seconds can be encoded and inserted into the serial code formats or translated from the input codes. These particular capabilities, although not listed would most likely be used in conjunction with one or more of the other options.

A-B-E CODE SELECT (13) (OPTION)

The Code Select option is used whenever multi code translation is required. Whenever the option is installed in the unit, a front panel switch allows the operator to select the IRIG code (A, B and or E) the unit is to translate.

ADVANCE/RETARD (20) (OPTION)

When in the generator mode of operation this assembly, in conjunction with front panel switches, allows the operator to slew the internally generated update clock in order to align it with an external reference signal.

EXTERNAL START (25) (OPTION)

Allows the unit to be started "on time" from an external WWV TICK signal or a DC pulse.

17 BIT BINARY CONVERTER (27) (OPTION)

Provides parallel buffered 17 bit Binary outputs (seconds, minutes, hours) of the major time counter. 10 bits of Binary milliseconds can also be provided.

SLOW CODE (29) (OPTION)

Converts parallel BCD information (major time), in conjunction with a front panel switch, to a bi-level 5 rate serial Slow Code format.

PARALLEL OUTPUTS (30) (OPTION)

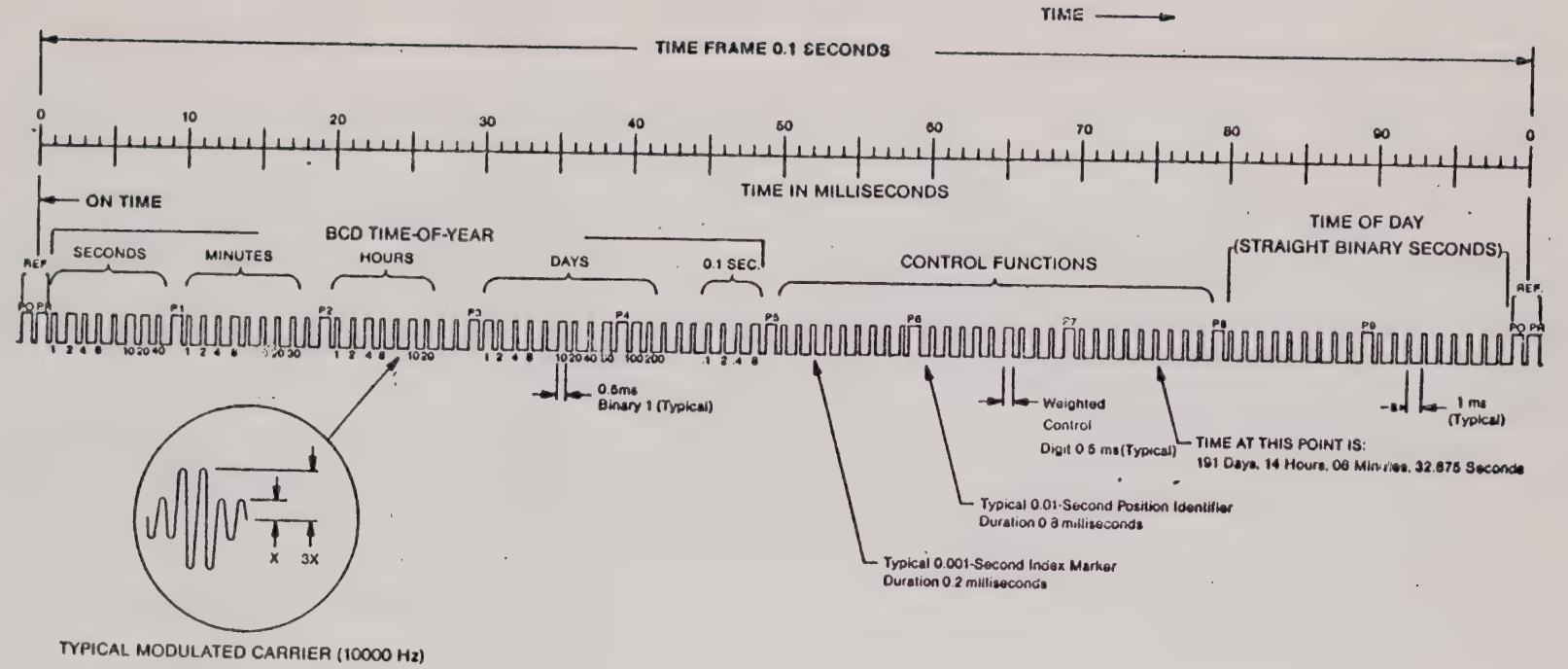
Provides parallel buffered BCD outputs of the major and or minor time counter contents. Also provides for other output timing signals and for external control of the Time Code Translator (e.g. Tape Search Control) if required.

IRIG A ENCODER (31) (OPTION)

This option provides for the generation of the IRIG A Time Code Format (A132). The operation of this assembly is the same as for IRIG B (32). However, since the code rate is 1000 PPS the input timing terms are different and the pulse widths mentioned are decreased by a factor of ten.

IRIG E ENCODER (35) (OPTION)

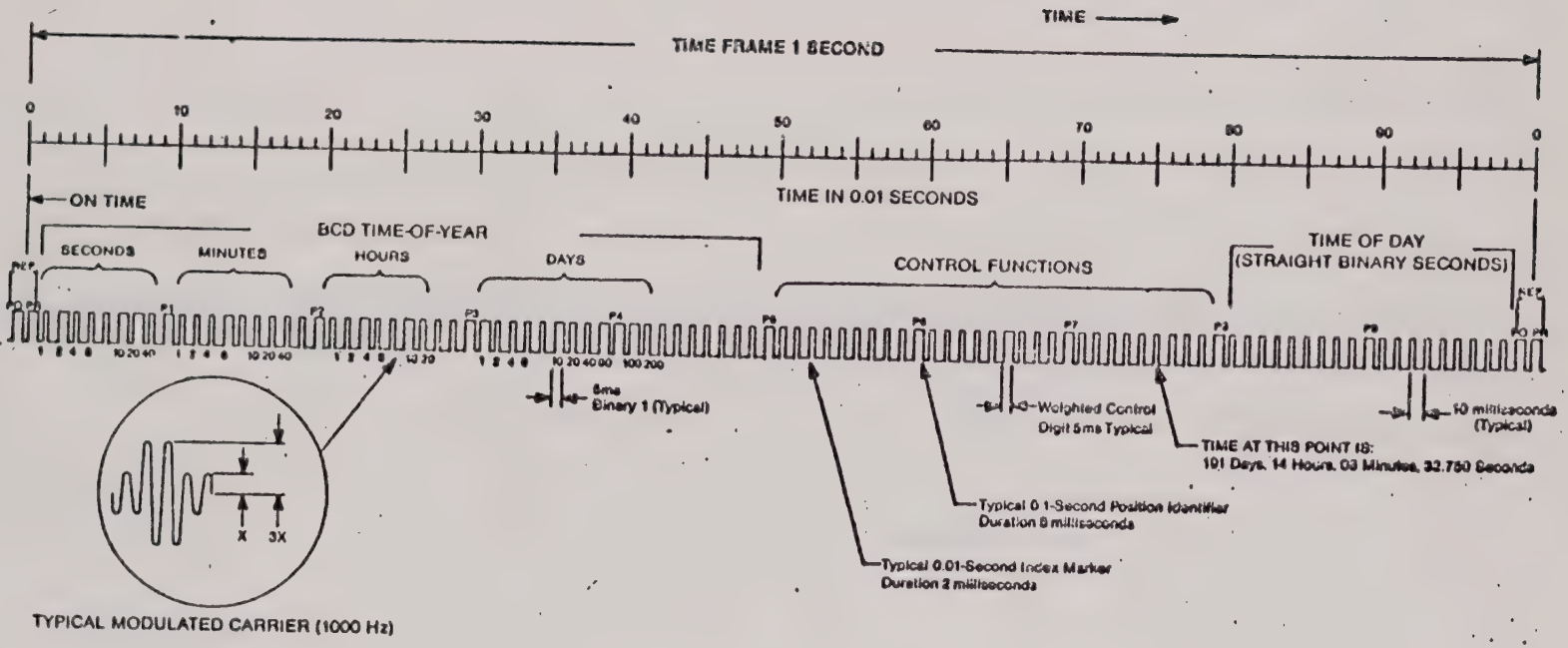
This option provides for the generation of an IRIG E Time Code Format (E112). The operation of this assembly is the same as for IRIG B (32). However, since the code rate is 10 PPS the input timing terms are different and the pulse widths are increased by a factor of ten.



IRIG STANDARD FORMAT A
SIGNAL A00
1000 PPS CODE
REFERENCE IRIG DOCUMENT 104-70

IRIG FORMAT 'A' – GENERAL

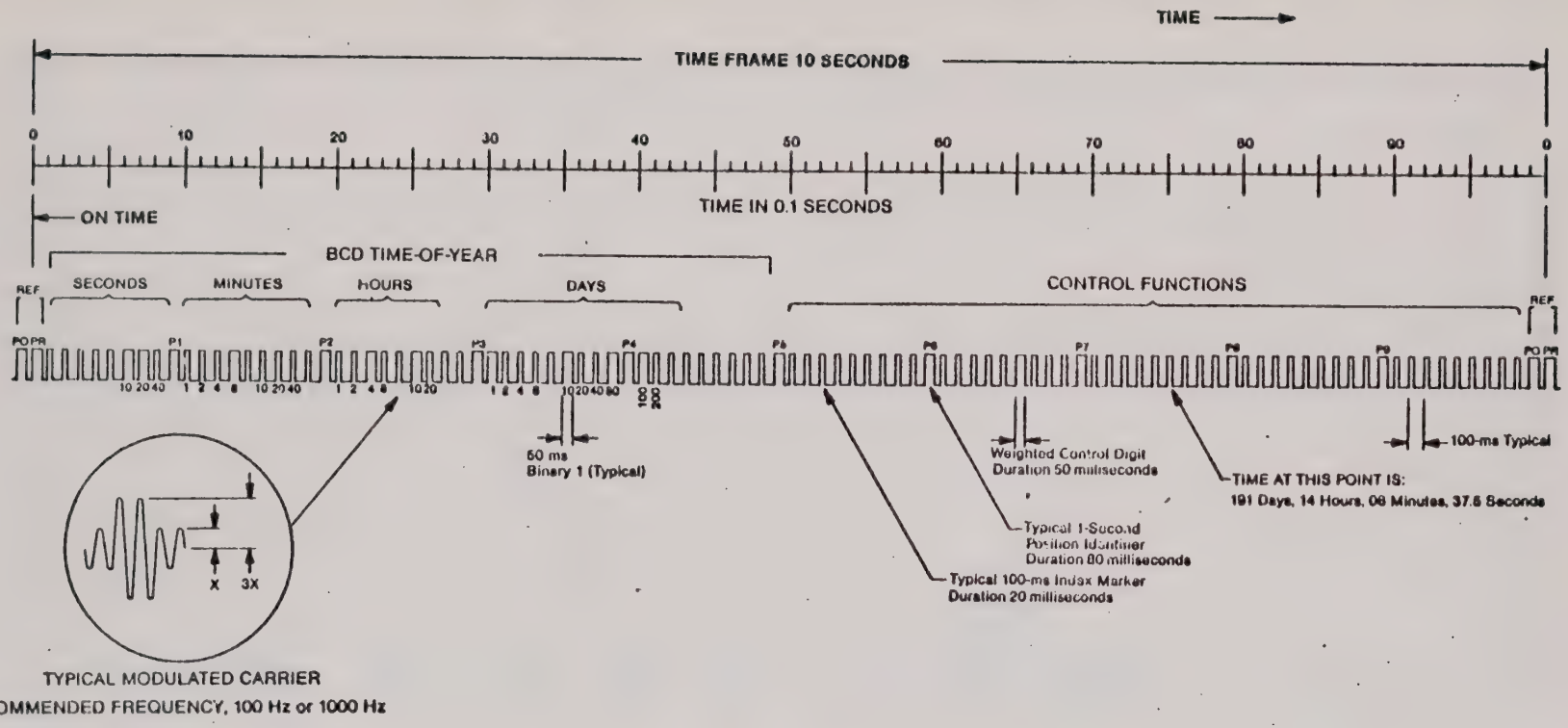
1. **TIME FRAME:** 0.1 second
2. **CODE DIGIT WEIGHTING OPTIONS:** BCD, SB or both:
   a. Binary Coded Decimal Time-of-Year CODE WORD — 34 binary digits.
      (1) Seconds, minutes, hours, days and 0.1 seconds. Recycles yearly.
   b. Straight Binary Time-of-Day CODE WORD — 17 binary digits.
      (1) Seconds only. Recycles each 24 hours. (86399)
3. **CODE WORD STRUCTURE:**
   a. **BCD.** Word begins at INDEX COUNT 1. Binary-coded elements occur between POSITION IDENTIFIER ELEMENTS (seven for seconds; seven for minutes; six for hours; ten for days; four for 0.1 seconds) until the CODE WORD is complete. A POSITION IDENTIFIER occurs between decimal digits in each group to provide separation for visual resolution.
   b. **SB.** Word begins at INDEX COUNT 80. Seventeen binary-coded elements occur, with a POSITION IDENTIFIER between the 9th and 10th binary-coded elements.
4. **LEAST SIGNIFICANT DIGIT:** Occurs first, except for fractional seconds information, which occurs following the day-of-year information.
5. **ELEMENT RATES AVAILABLE:**
   a. 1000 per second (basic Element rate)
   b. 100 per second (POSITION IDENTIFIER rate)
   c. 10 per second (Frame rate)
6. **ELEMENT IDENTIFICATION:**
   a. "On-Time" reference point for each Element is its leading edge.
   b. INDEX MARKER duration: 0.2 milliseconds (Binary Zero or uncoded Element)
   c. CODE DIGIT duration: 0.5 milliseconds (Binary one)
   d. POSITION IDENTIFIER: 0.8 milliseconds
   e. REFERENCE MARKER: Two consecutive POSITION IDENTIFIERS.
   (The "on-time" point, to which the CODE WORD refers, is the leading edge of the second POSITION IDENTIFIER.)
7. **RESOLUTION:** 1 millisecond (unmodulated); 0.1 millisecond (modulated).
8. **CARRIER FREQUENCY:** 10 kHz when modulated.



IRIG FORMAT 'B'—GENERAL

1. **TIME FRAME:** 1.0 second.
2. **CODE DIGIT WEIGHTING OPTIONS:** BCD, SB or both:
   a. Binary Coded Decimal Time-of-Year CODE WORD — 30 binary digits.
      (1) Seconds, minutes, hours and days. Recycles yearly.
   b. Straight Binary Time-of-Day CODE WORD — 17 binary digits.
      (1) Seconds only. Recycles each 24 hours. (86399)
3. **CODE WORD STRUCTURE:**
   a. **BCD:** Word begins at INDEX COUNT 1. Binary-coded elements occur between POSITION IDENTIFIER ELEMENTS (seven for seconds, seven for minutes; six for hours; ten for days) until the CODE WORD is complete. A POSITION IDENTIFIER occurs between decimal digits in each group to provide separation for visual resolution.
   b. **SB:** Word begins at INDEX COUNT 80. Seventeen binary-coded elements occur with a POSITION IDENTIFIER between the 9th and 10th binary-coded elements.
4. **LEAST SIGNIFICANT DIGIT:** occurs first.
5. **ELEMENT RATES AVAILABLE:**
   a. 100 per second (basic Element rate)
   b. 10 per second (POSITIVE IDENTIFIER Rate)
   c. 1 per second (Frame Rate)
6. **ELEMENT IDENTIFICATION:**
   a. "On-Time" reference point for each Element is its leading edge.
   b. INDEX MARKER duration: 2 milliseconds (Binary zero or uncoded Element)
   c. CODE DIGIT duration: 5 milliseconds (Binary one)
   d. POSITION IDENTIFIER duration: 8 milliseconds
   e. REFERENCE MARKER — one per second: Two consecutive POSITION IDENTIFIERS.
      (The "On-Time" point, to which the CODE WORD refers, is the leading edge of the second POSITION IDENTIFIER.)
7. **RESOLUTION:** 10 milliseconds (unmodulated); 1 millisecond (modulated).
8. **CARRIER FREQUENCY:** 1 kHz when modulated.

IRIG STANDARD FORMAT B
SIGNAL B00
100 PPS CODE
REFERENCE IRIG DOCUMENT 104-70



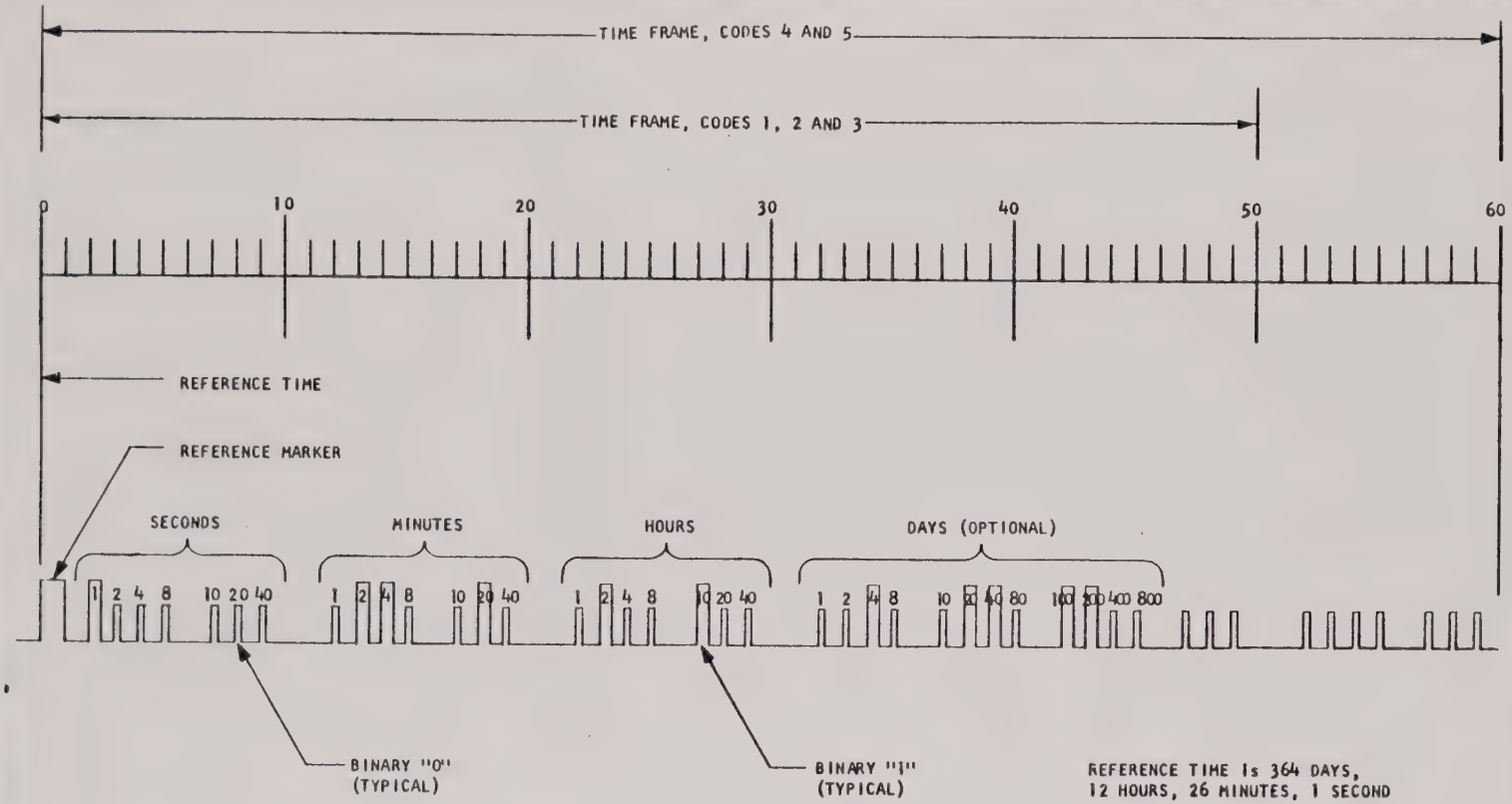
TYPICAL MODULATED CARRIER
RECOMMENDED FREQUENCY, 100 Hz or 1000 Hz

IRIG FORMAT 'E' — GENERAL

1. **TIME FRAME:** 10 seconds
2. **CODE DIGIT WEIGHTING:** BCD: Time-of-Year CODE WORD — 26 Binary Digits. Seconds, minutes, hours and days; recycles yearly.
3. **CODE WORD STRUCTURE:**
   BCD: Word begins at INDEX COUNT 6. Binary-coded Elements occur between POSITION IDENTIFIER ELEMENTS (three for seconds, seven for minutes; six for hours, ten for days) until the CODE WORD is complete. A POSITION IDENTIFIER occurs between decimal digits in each group to provide separation for visual resolution.
4. **LEAST SIGNIFICANT DIGIT:** Occurs first.
5. **ELEMENT RATES AVAILABLE:**
   a. 10 per second (basic Element rate)
   b. 1 per second (POSITION IDENTIFIER Rate)
   c. 0.1 per second (Frame Rate)
6. **ELEMENT IDENTIFICATION:**
   a. "On-Time" reference point for each Element is its leading edge.
   b. INDEX MARKER duration: 20 milliseconds (Binary zero or uncoded Element)
   c. CODE DIGIT duration: 50 milliseconds (Binary one)
   d. POSITION IDENTIFIER duration: 80 milliseconds (Refers to the leading edge of the succeeding Element).
   e. REFERENCE MARKER (one per 10 seconds): Two consecutive POSITION IDENTIFIERS.

   (The "On-Time' point, to which the CODE WORD refers, is the leading edge of the second POSITION IDENTIFIER.)
7. **RESOLUTION:** 100 milliseconds (unmodulated); 1 millisecond (modulated).
8. **CARRIER FREQUENCY:** 1 kHz or 100 Hz when modulated.

IRIG STANDARD FORMAT E
SIGNAL E00
10 PPS CODE
REFERERCE IRIG DOCUMENT 104-70



CODE	PULSE RATE	FRAME PERIOD	BINARY ZERO	BINARY ONE	FRAME REFERENCE PULSE
1	50 PPS	1 SEC	4 MS	10 MS	20 MS
2	10 PPS	5 SEC	20 MS	50 MS	100 MS
3	5 PPS	10 SEC	40 MS	100 MS	200 MS
4	1 PPS	60 SEC	200 MS	500 MS	1,000 MS
5	1 PPS IOS	10 MIN	2 SEC	5 SEC	10 SEC

datum inc.

BI-LEVEL SLOW CODE REV. A

SECTION VI
MAINTENANCE

The 9300 Time Code Generator/Translator utilizes integrated circuits. There are no moving parts or parts with limited life. There is no periodic maintenance required for the unit under normal conditions. If the unit is exposed to unusual operating conditions such as high dust or high humidity environments, or if the unit is dropped or otherwise damaged, it may be necessary to perform certain inspections and/or repairs.

If it is necessary to inspect the unit, the following should be considered:

1. Always disconnect AC power before removing the instrument cover. To remove the cover, simply remove the screw at the rear panel and slide the cover off to the rear.

2. Make a thorough visual inspection of all circuitry and wiring.

3. Check for physical integrity of all components. Look for burned or cracked components, loose physical damage, leakage of insulation compounds or general physical damage. To aid in overall maintenance and repair, each integrated circuit is mounted in an individual modular socket. Removal or replacement is therfore convenient and easy.

   It should rarely be necessary to replace an integrated circuit; however, if replacement is attempted, be sure that all component leads enter the socket and that no leads are bent under the component or extended out from the socket.

   Check to see that all IC's are firmly mounted in the socket so that good electrical contact is made.

4. Check all switches and connectors for loose or broken wires.

5. If the internal component surfaces and components have an excessive amount of dust deposited on them, use a soft brush and a low pressure stream of air to remove any foreign material.

CAUTION

Do not clean PC boards or small internal components with a stiff brush or solvents since damage to the circuits may result. A high powered vacuum cleaner device should not be used on small internal components.

6. Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints and other foreign material.

7. Replace the cover and reconnect the AC power and input connector. Check operation. If performance does not match or exceed the specifications listed, corrective maintenance is in order.

Printed Circuit Board Repair

Removal and insertion of IC components can be easily made as described above. Should it be necessary to replace conventional components which are soldered to the circuit board, cut the leads of the part near the lead holes. Using a low power (50 watts or less) soldering iron, apply heat sparingly to each cut lead. As soon as the solder melts, slip the lead from the hole and clean the hole with a tooth pick. Clean the board surfaces with isopropyl alcohol. Form the tinned leads of the replacement part and insert in cleaned holes, trimming the leads to extend 1/16-inch beyond the back surface of the board. Only 63/37 solder with a maximum

diameter of 1/16 inch should be used. Solder the leads to the board and use a hemostat, long nosed pliers, or other heat sink on the leads of all semiconductor devices and quarter-watt resistors. Allow the soldered junction to cool before removing the heat sink.

WARNING

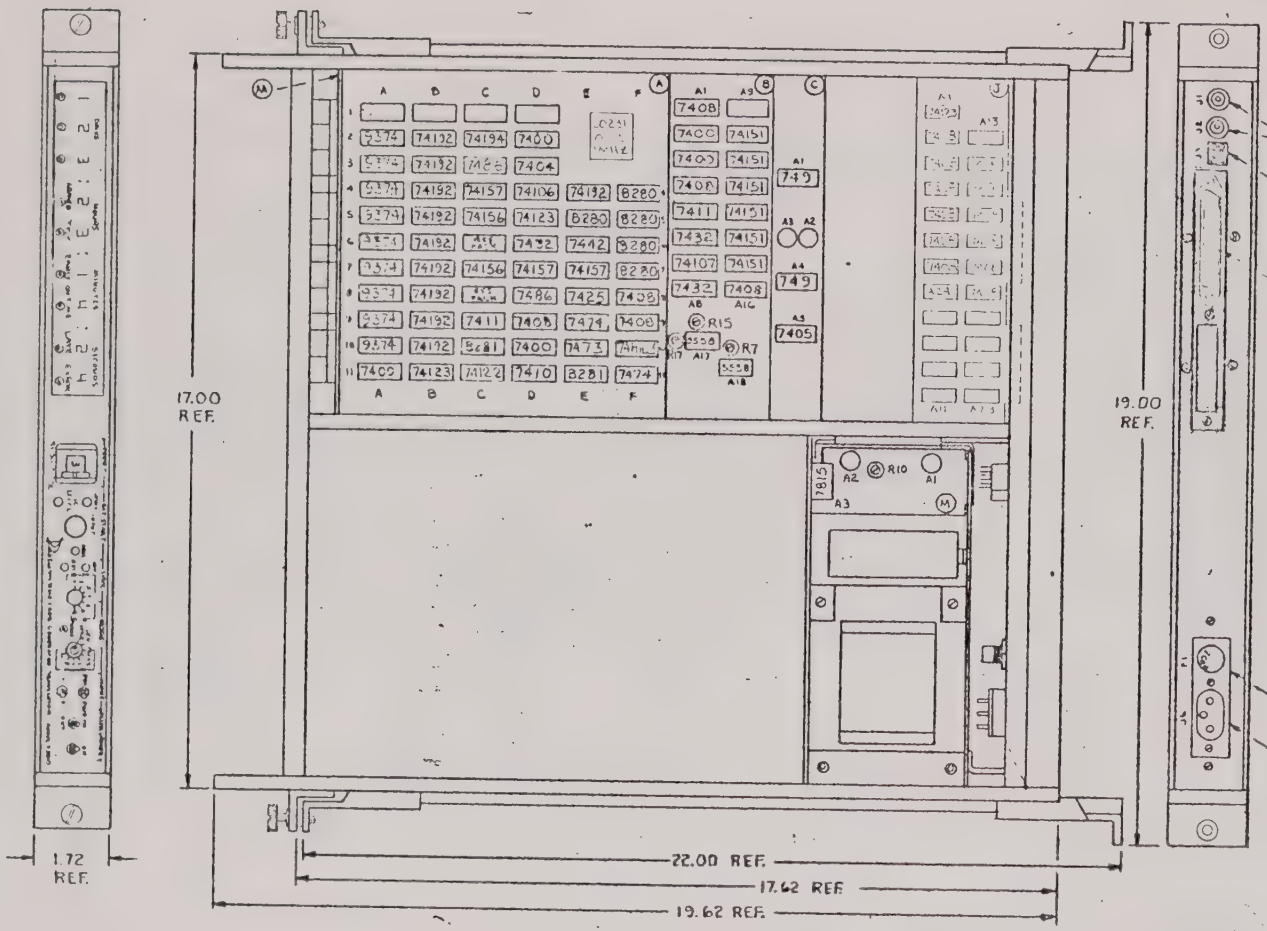
Dangerous high voltages are present in the unit. Use caution at all times when the protective cover is removed.

SECTION VII

LIST OF DRAWINGS

1.	Top Assembly	9300-708
2.	AGC (1)	16085
3.	IRIG Basic (2) (3) (4) (5) (7) (8) (9) (10)	16543
4.	Switch & Control Logic (11)	9300-8108
5.	LED Display (12)	16549
6.	Parallel Outputs (30)	16635
7.	IRIG B Encoder (32)	16062
8.	Power Supply (49)	16280
9.	Wiring Diagram	803485

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



(M) 16280-3 POWER SUPPLY
(1) 16635-123 PARALLEL OUTPUTS
(C) 16085 AGC
(B) 16062-1 IRIG B ENCODER
(A) 16543-13 BASIC
2 (M) 16549-1 DISPLAY
1. TOP COVER REMOVED FOR CLARITY.

NOTES: UNLESS OTHERWISE SPECIFIED

7. SWITCH & CONTROL LOGIC 9300-8108
6. WIRING DIA - 803485 (BASIC)
5. WIRE LIST - 803486 (BASIC), 803589 (PARALLEL OUTPUTS)
J6 - AC POWER INPUT
J5 -
J4 - PARALLEL OUTPUTS (MS, SMHD)
J3 - PULSE RATES
J2 - CODE OUTPUT } IRIG B
4. J1 - CODE INPUT }
3 SLIDES & REAR MTG BRKTS ARE OPTIONAL

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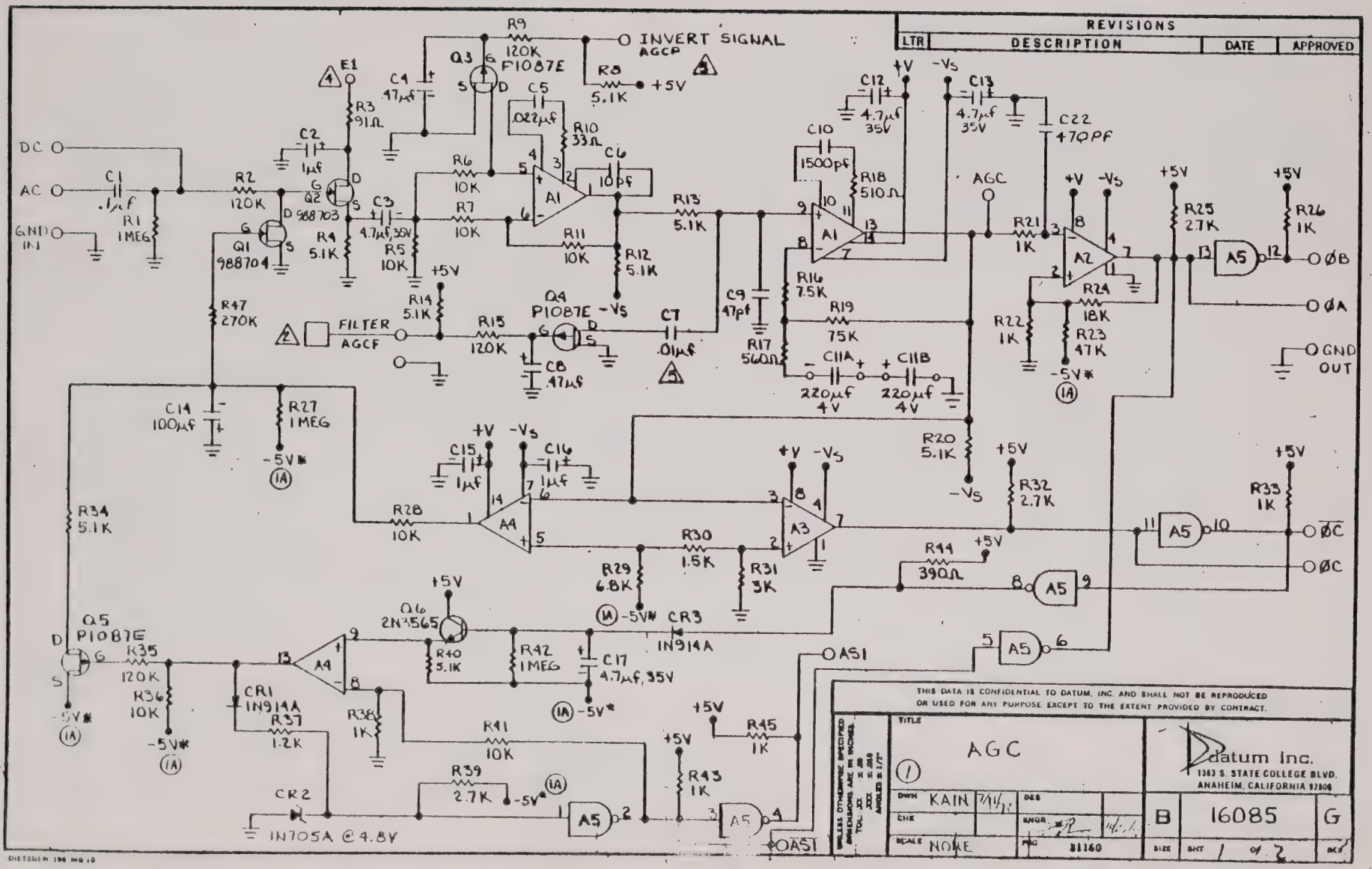
TITLE: TIME CODE GENERATOR/TRANSLATOR

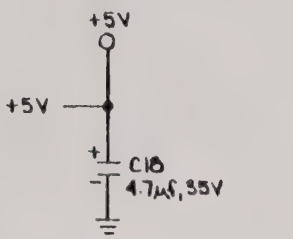
Datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

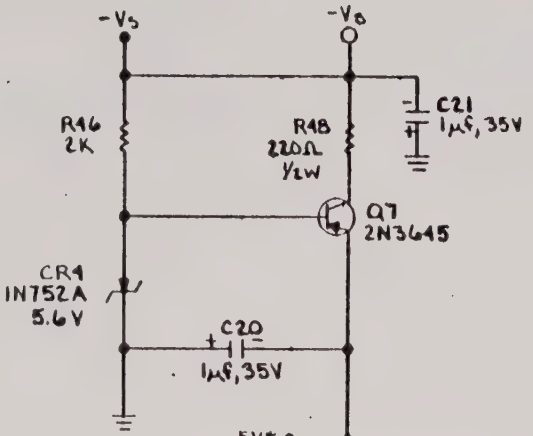
C 9300-708

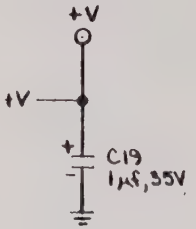
DWG | ENG | CHK | MFG | QUAL NONE | TEST | SIZE C | SCALE | WT | SHT 1 OF 1 | REV


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
INVERT SIGNAL
AGCP
DC
AC
GND IN
FILTER
AGCF
AGC
GND OUT
ØB
ØA
ØC
ØC
AS1
AS1
-5V*
+5V
+V
-Vs
IN705A @4.8V
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°
TITLE
AGC
(1)
DWN KAIN 7/14/72
CHK
ENGR
SCALE NONE
DWG 81160
SIZE B
16085
G
SHT 1 OF 2
datum inc.
1303 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ADDED C22	9-27-72	R.F.
B	ADDED R20 TO SCHEMATIC +E WAS +Vs	1-22-73	RM
C	Q3,4,5 WERE 2N4342	6-13-73	R.J.
D	ADDED C11A & C11B	7-13-73	RM
E	Q1 WAS 988703	9-12-73	R.J./C.V
F	C12 & C13 WERE 1 μf	9-21-73	RM/C.V
G	R3 WAS TO +E, ADDED E1	11-26-73	RM/R.S.







5 -1 C7 IS .001μf.

1 WIRE TO +15 OR +5V AS REQUIRED

3 THIS POINT GROUNDED TO INVERT SIGNAL - REVERSE MODE

2 SEE PARALLEL OUTPUT SCHEM FOR PIN NUMBER

1 REMOVE FOR REMOTE OR HIGHSPEED OPERATION

PART NO	MFR	REF
SN7405	NATIONAL	A5
μA749	FAIRCHILD	A1, A4
LM311H	NATIONAL	A2, A3

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.010 .XXX ±.005 ANGLES ±1/2°

TITLE: AGC

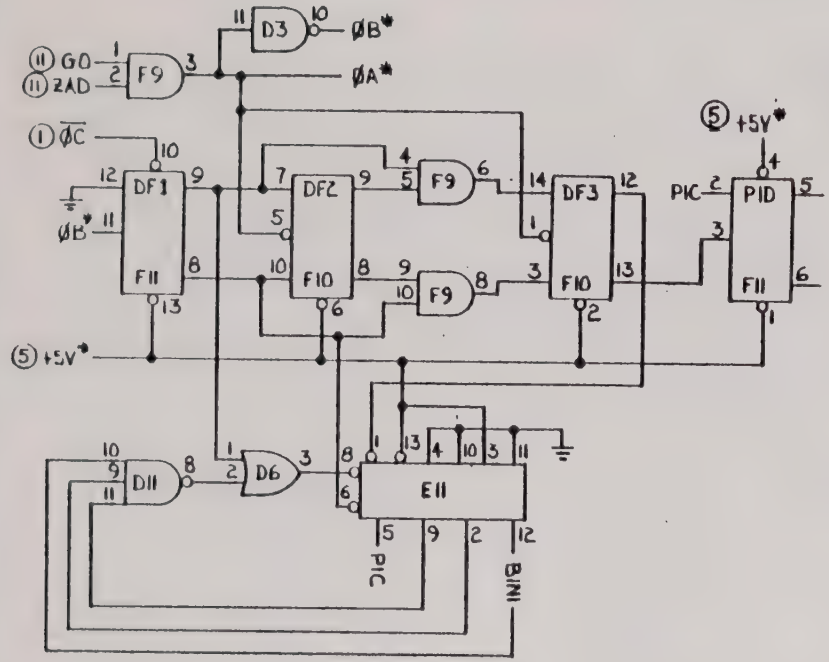
(1A)

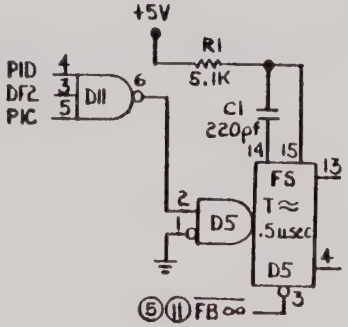
DWN KAIN 7/12/72 | DES RF 7/12/72 | CHK | ENGR | SCALE NONE | FSC 31160

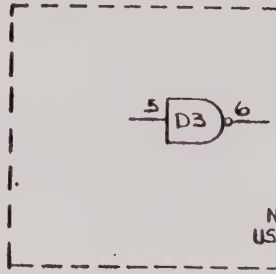
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

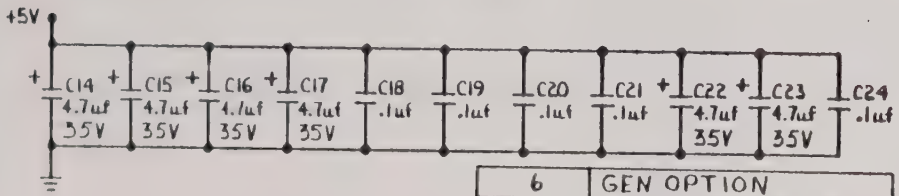
B | 16085 | G

SIZE | SHT 2 OF 2 | REV









REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

PART NO	MFR	REF DES
899-1-R6K	BECKMAN	C6, C8
LM311D	NATIONAL	A1
MC12061P	MOTOROLA	D1
9374-DC	FAIRCHILD	A2-A10
N82B1A	SIGNETICS	C10, E11
N82B0A	SIGNETICS	E5, F4-F7, C1
N7486A	↕	C3, D8
N7473A	↕	E10
N7442B	SIGNETICS	E6
SN7432N	T.I.	D6
N7411A	SIGNETICS	C9
N7410A	↕	D11
N7408A	↕	D9, F8, F9
N7404A	↕	D3
N7400A	SIGNETICS	D2, D10, A11
SN74156N	T.I.	C5, C7
SN7474N	↕	E9, F11
SN7425N	↕	E8
SN74194N	↕	C2
SN74192N	↕	B2-B10, E4
SN74157N	↕	C4, D7, E7
SN74123N	↕	D5, B11
SN74H106N	↕	D4
SN74H103N	T.I.	F10
SN74122N	TI	C11

PART NO	MFR	REF DES

DASH NO	DESCRIPTION
6	GEN OPTION
5	10MHZ CRYSTAL OSC
4	CO251 OSC
3	CO231 OSC
2	EXT OSC
1	DAYS
—	BASIC S-M-H

NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.02 .XXX ±.010 ANGLES ±1/2°

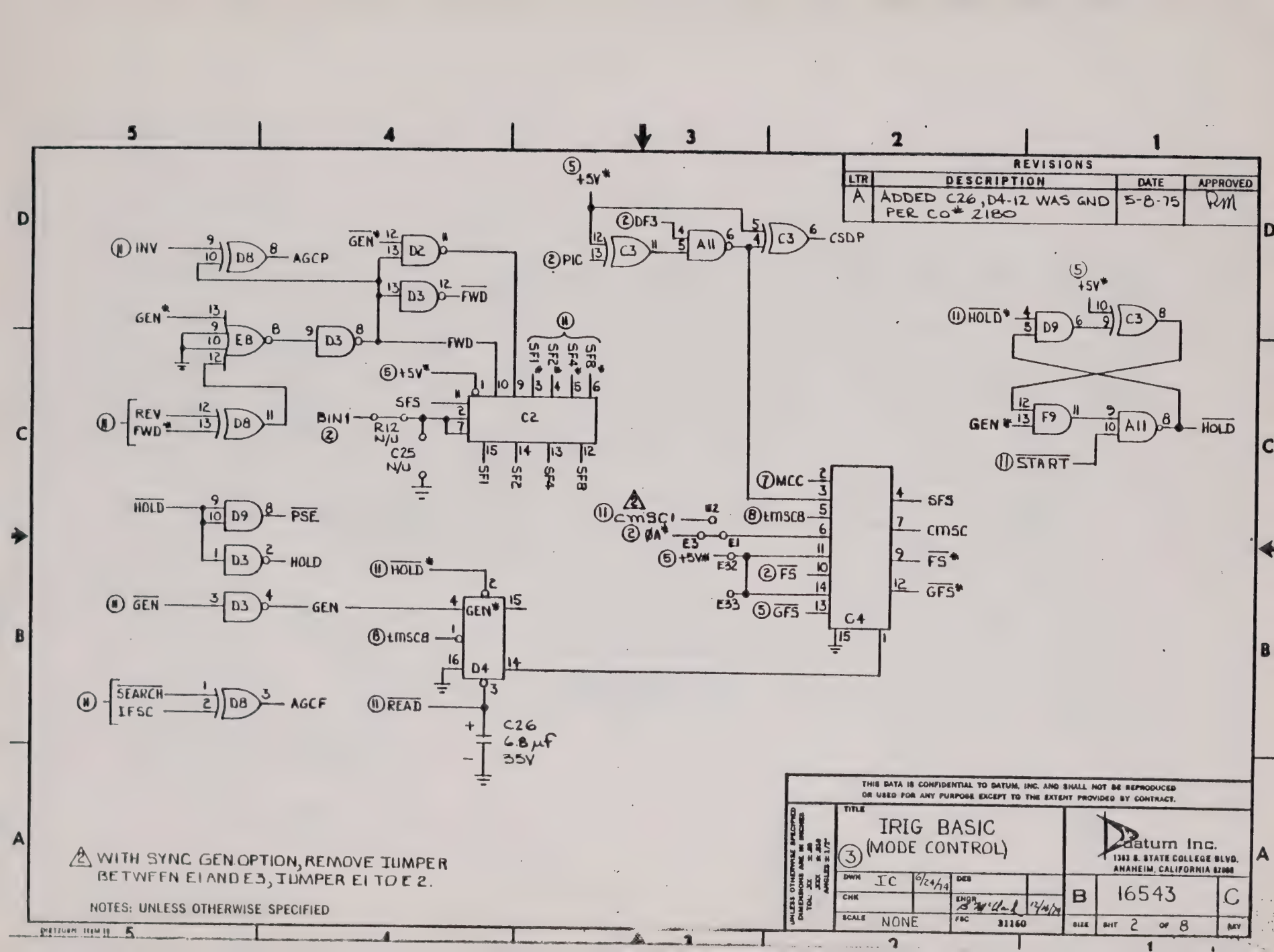
TITLE: IRIG BASIC (2) (DECODER)

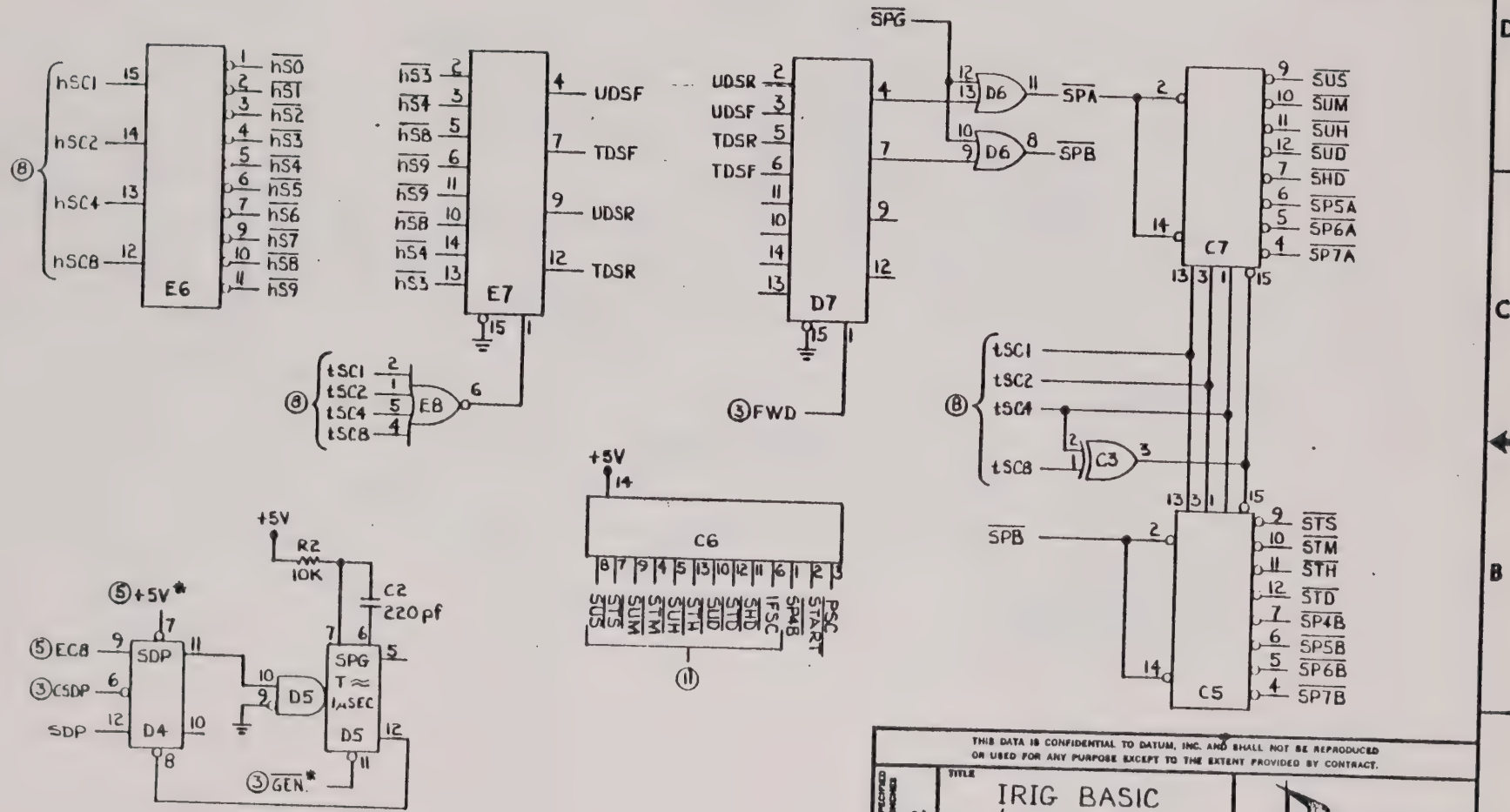
DWN	IC	6/24/74	DES
CHK			ENGR
SCALE	NONE		FSC 33160

Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

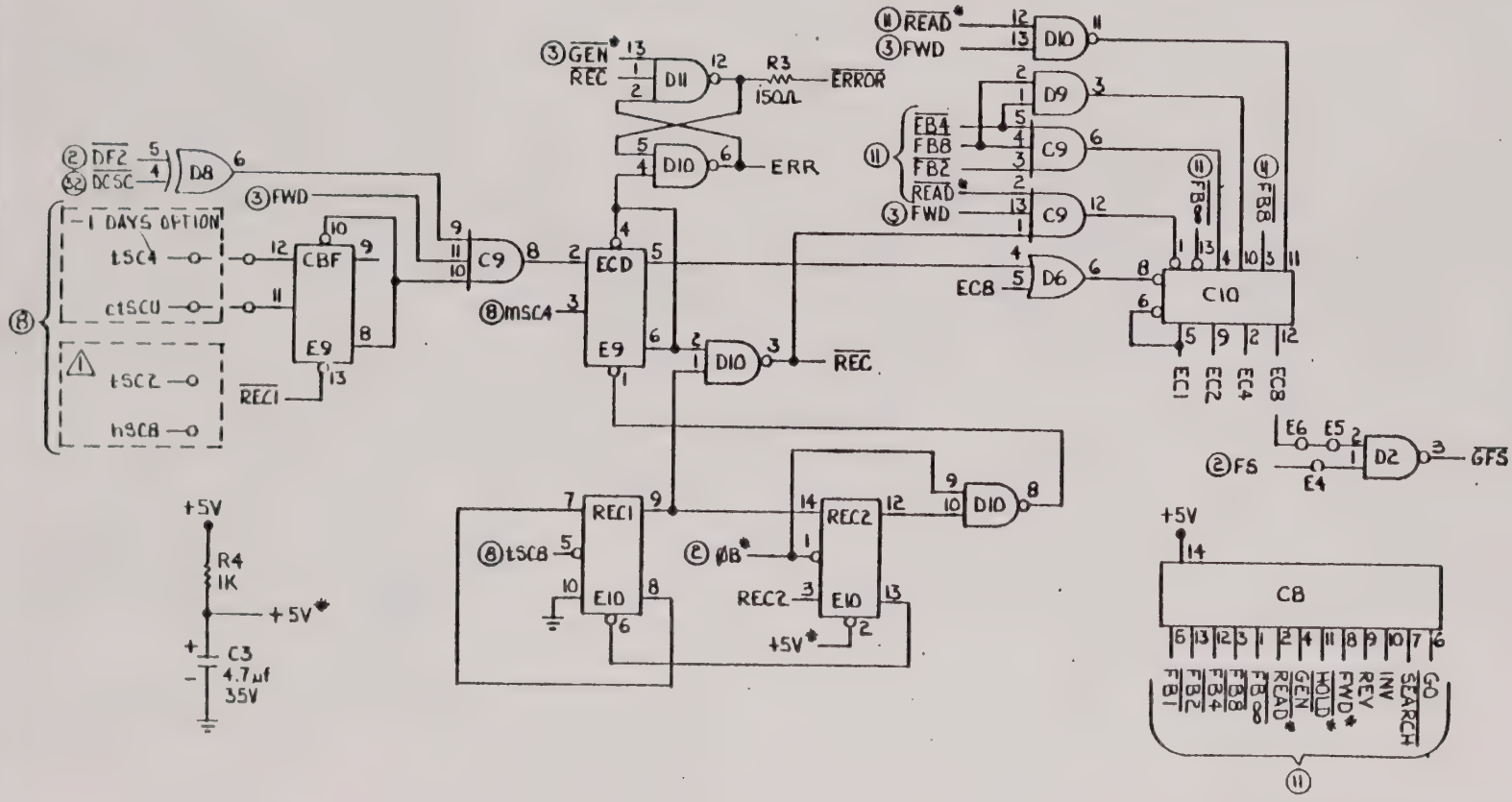
SIZE B | 16543 | REV C

SHT 1 OF 8


REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
A | ADDED C26, D4-12 WAS GND PER CO# 2180 | 5-8-75 | RM
INV
AGCP
GEN*
FWD
REV
FWD*
BIN1
R12 N/U
C25 N/U
SFS
C2
SF1
SF2
SF4
SF8
+5V*
PIC
DF3
CSDP
HOLD*
START
HOLD
PSE
GEN
SEARCH
IFSC
AGCF
READ
C26
6.8µf
35V
MCC
tmSC8
tmSC1
ØA*
+5V*
FS*
GFS*
SFS
CMSC
C4
D4
WITH SYNC GEN OPTION, REMOVE JUMPER BETWEEN E1 AND E3, JUMPER E1 TO E2.
NOTES: UNLESS OTHERWISE SPECIFIED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
TITLE
IRIG BASIC
(3) (MODE CONTROL)
DWN IC 6/24/74
CHK
ENGR 11/10/74
SCALE NONE
FSC 31160
Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
B 16543 C
SIZE SHT 2 OF 8 REV


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
E6
E7
E8
D4
D5
D6
D7
C2
C3
C5
C6
C7
R2
10K
220pf
+5V
SPG
UDSF
TDSF
UDSR
TDSR
FWD
GEN.*
SDP
CSDP
ECB
SPA
SPB
T ≈ 1μSEC
PSC START
IRIG BASIC
(SCAN LOGIC)
datum Inc.
1343 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
NOTES: UNLESS OTHERWISE SPECIFIED
DWN IC 6/24/74
CHK
ENGR 12/4/74
SCALE NONE
FSC 81160
B
16543
C
SHT 3 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



⚠ IF DAYS OPTION IS NOT SUPPLIED:
E9-12 IS CONNECTED TO tSC2
E9-11 IS CONNECTED TO hSC8

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TITLE: IRIG BASIC (SYNC MODE) (5)

DWN IC 6/25/74 DES

CHK ENGR 12/16/74

SCALE NONE FSC 33160

Datum Inc.
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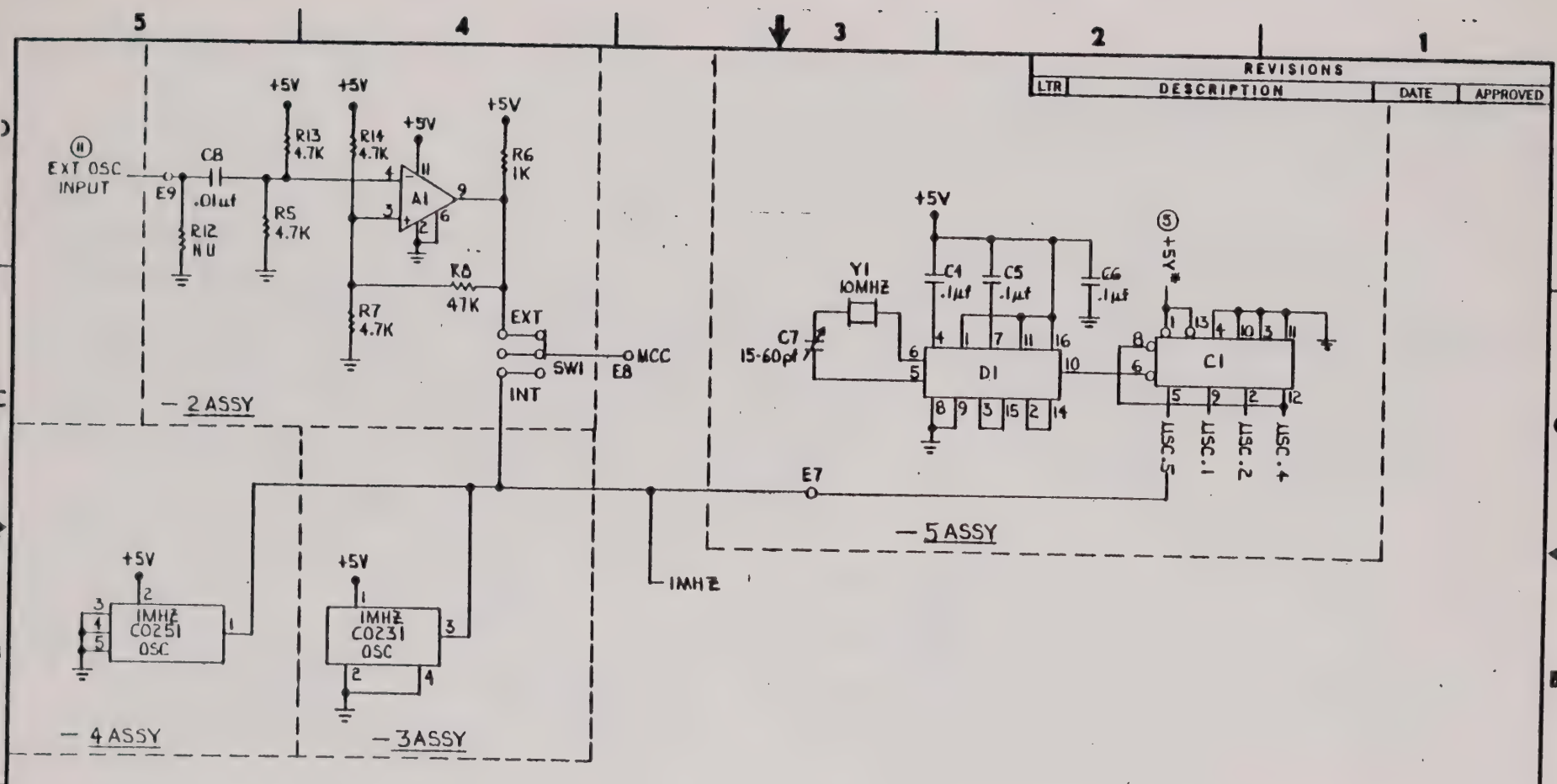
B 16543 C

SIZE SHT 4 OF 8 REV



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

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TITLE: IRIG BASIC (TIME BASE) (7)

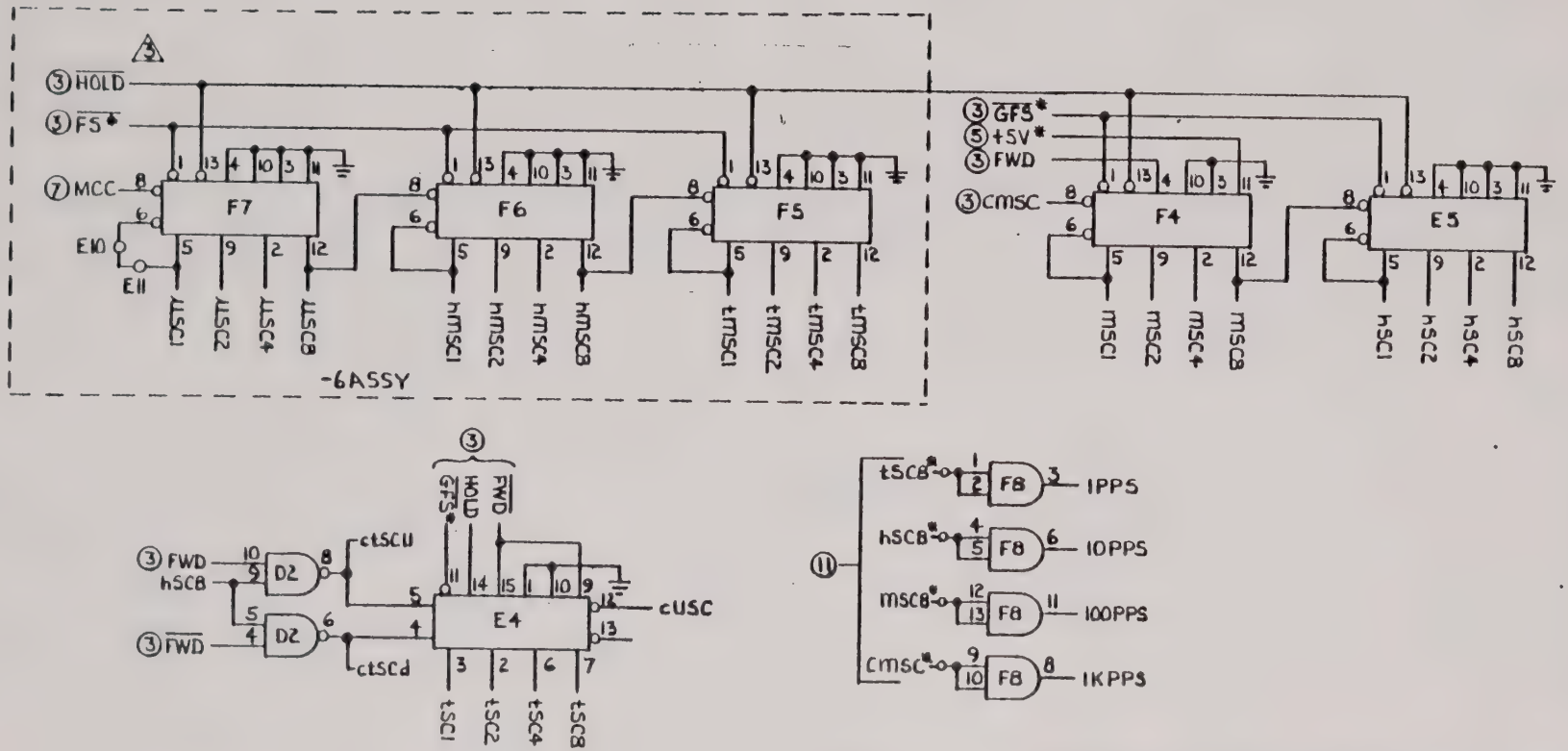
DWN	IC	6/25/74	DES
CHK			ENGR
SCALE	NONE		FSC 31168

Datum Inc. 1363 S. STATE COLLEGE BLVD. ANAHEIM, CALIFORNIA 92806

B | 16543 | C

SIZE | SHT 5 OF 8 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
B	C11 WAS 74123 PER CO*2277	9-9-75	Phil
C	REVISED PER C.O. 2747	6-18-76	IC



⚠2 WHEN SYNC GEN OPTION IS USED ALL -6 TERMS ORIGINATE ON ⑮

NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: IRIG BASIC ⑧ (MINOR TIME)

DWN	IC	6/25/74	DES	
CHK			ENGR	14/24/74
SCALE	NONE		FSC	21160

datum Inc.
1363 S. STATE COLLEGE BLVD.
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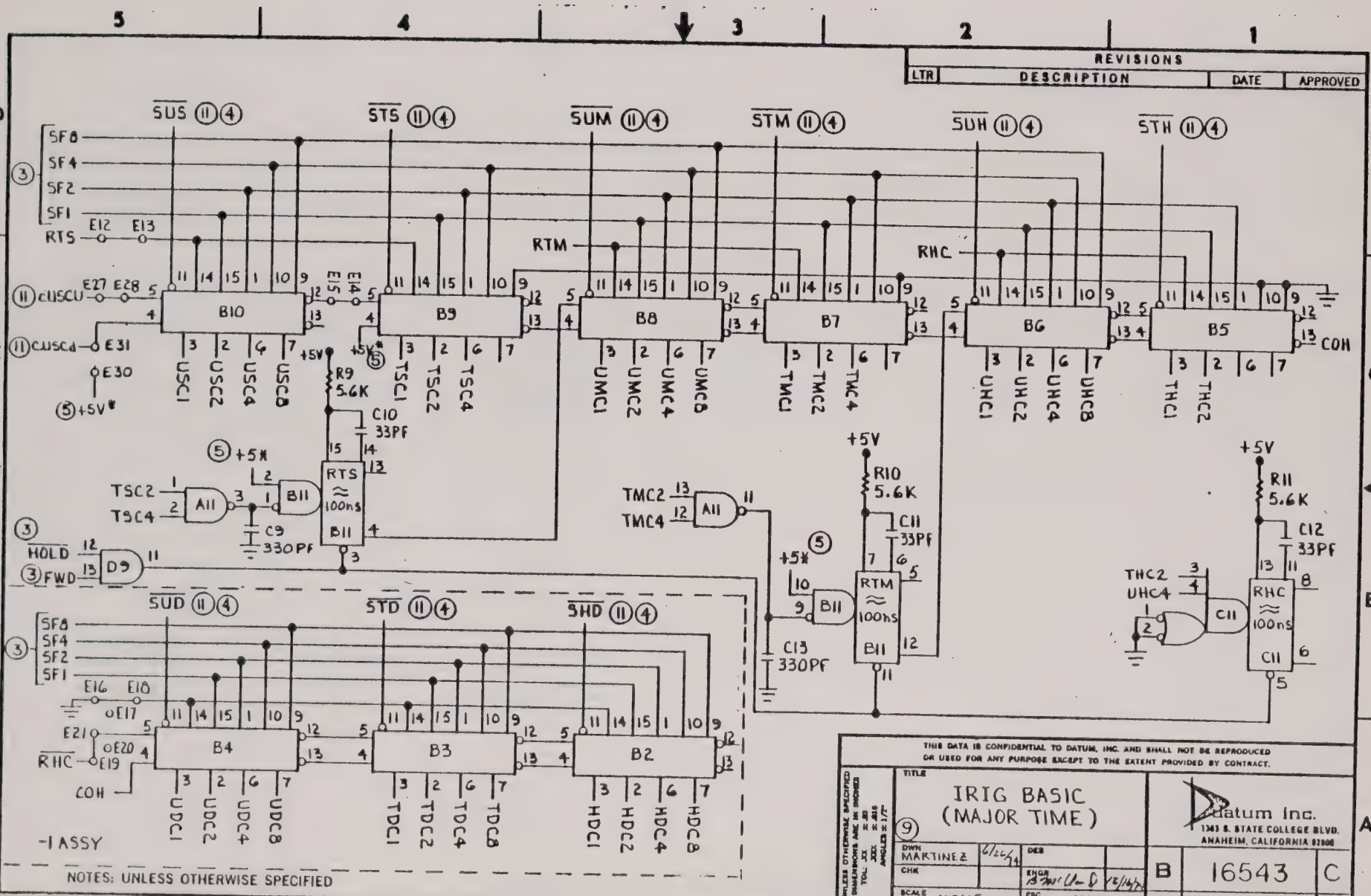
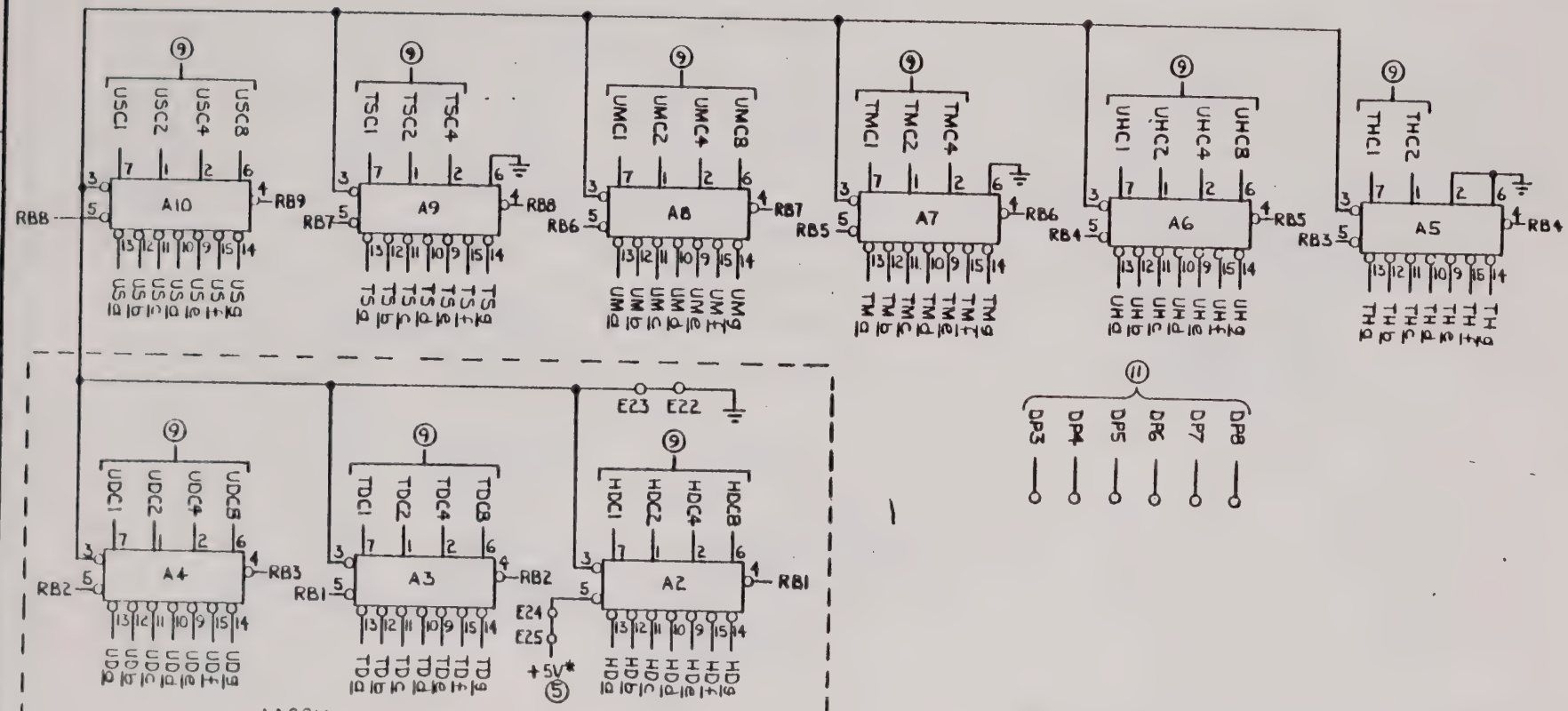
SIZE		SHT		REV
B	16543	6 OF 8		C


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
SUS ⑪④
STS ⑪④
SUM ⑪④
STM ⑪④
SUH ⑪④
STH ⑪④
SF8
SF4
SF2
SF1
RTS
RTM
RHC
E12
E13
E27
E28
E15
E14
E31
E30
+5V
R9 5.6K
C10 33PF
RTS ≈ 100ns
C9 330PF
TSC2
TSC4
A11
B11
HOLD
FWD
D9
R10 5.6K
C11 33PF
RTM ≈ 100ns
C13 330PF
TMC2
TMC4
R11 5.6K
C12 33PF
THC2
UHC4
C11
RHC ≈ 100ns
B10
B9
B8
B7
B6
B5
USC1
USC2
USC4
USC8
TSC1
TSC2
TSC4
UMC1
UMC2
UMC4
UMC8
TMC1
TMC2
TMC4
UHC1
UHC2
UHC4
UHC8
THC1
THC2
COH
SUD ⑪④
STD ⑪④
SHD ⑪④
E16
E18
E17
E21
E20
E19
B4
B3
B2
UDC1
UDC2
UDC4
UDC8
TDC1
TDC2
TDC4
TDC8
HDC1
HDC2
HDC4
HDC8
-1 ASSY
NOTES: UNLESS OTHERWISE SPECIFIED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
TITLE
IRIG BASIC (MAJOR TIME)
9
DWN MARTINEZ 6/26/74
CHK
ENGR 12/14/74
SCALE NONE
FSC 81160
Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
B
16543
C
SHT 7 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL. XXX ± .010
XX ± .030
ANGLES ± 1/2°

TITLE
IRIG BASIC
(10) (DISPLAY DRIVERS)

DWN	IC 6/25/74	DES	
CHK		ENGR	12/74
SCALE	NONE	FSC	31160

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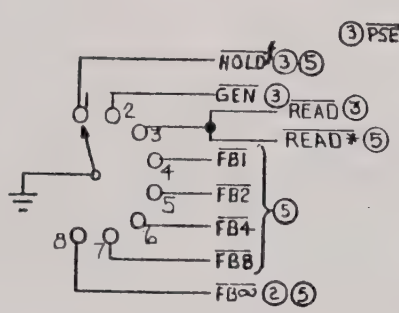
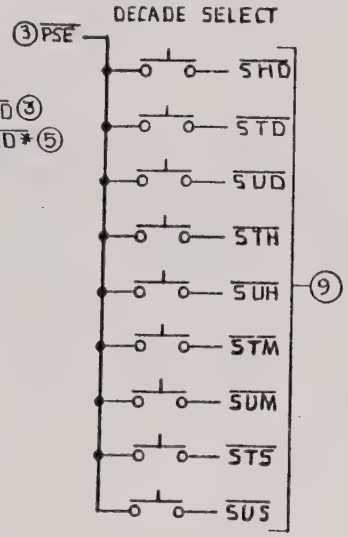
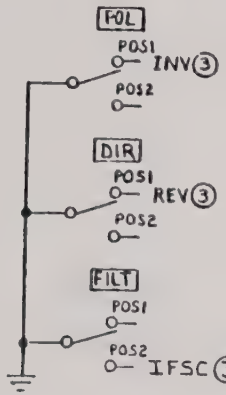
ANAHEIM, CALIFORNIA 92806

SIZE		SHT	OF	REV
B	16543	8	8	C

POS.	MODE SW.
1	HOLD
2	GEN
3	READ
4	FB1
5	FB2
6	FB4
7	FB8
8	FB∞



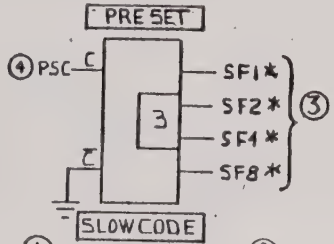


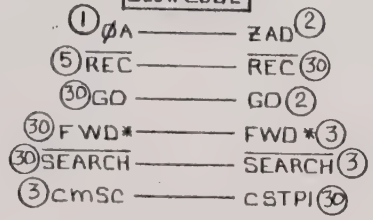


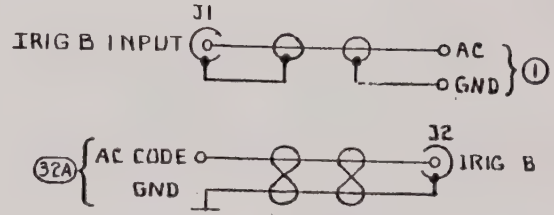
POL SW	
POS1	+
POS2	−

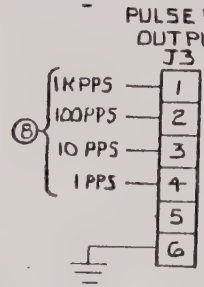
DIRECTION SW	
POS1	FWD
POS2	REV

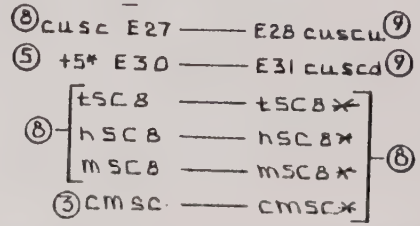
FILTER SW	
POS1	IN
POS2	OUT











TERMS (11) REFERENCED TO THIS PRINT AND NOT SHOWN ARE FOR INTERNAL REFERENCE ONLY

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

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TITLE: SWITCH & CONTROL LOGIC (11) (9300-708)

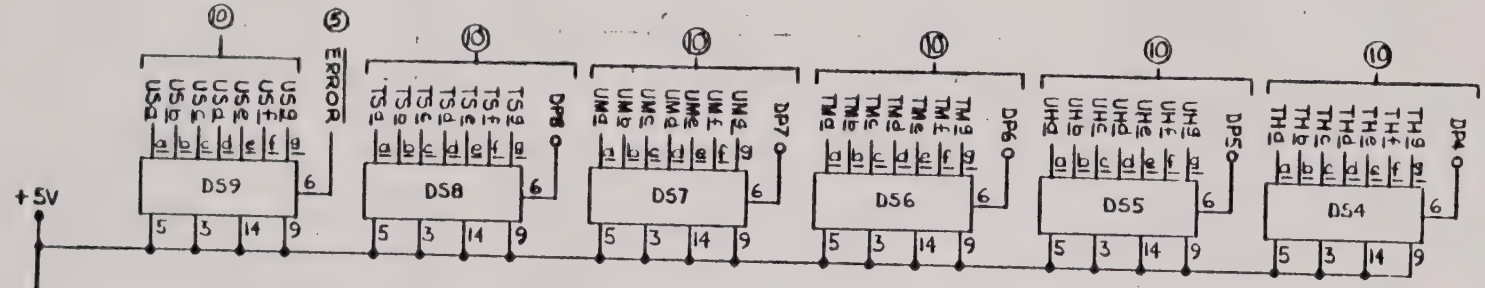
DWN	KAIN	1/8/75	DLS
CHK			
SCALE	NONE	FSC	23160

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B 9300-8108

SIZE SHT 1 OF 1 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



- 3 LEDS ARE FAIRCHILD FND-507
- 2 LEDS ARE MONSANTO MAN6A
1. LEDS ARE H/P 5082-7750

NOTES: UNLESS OTHERWISE SPECIFIED

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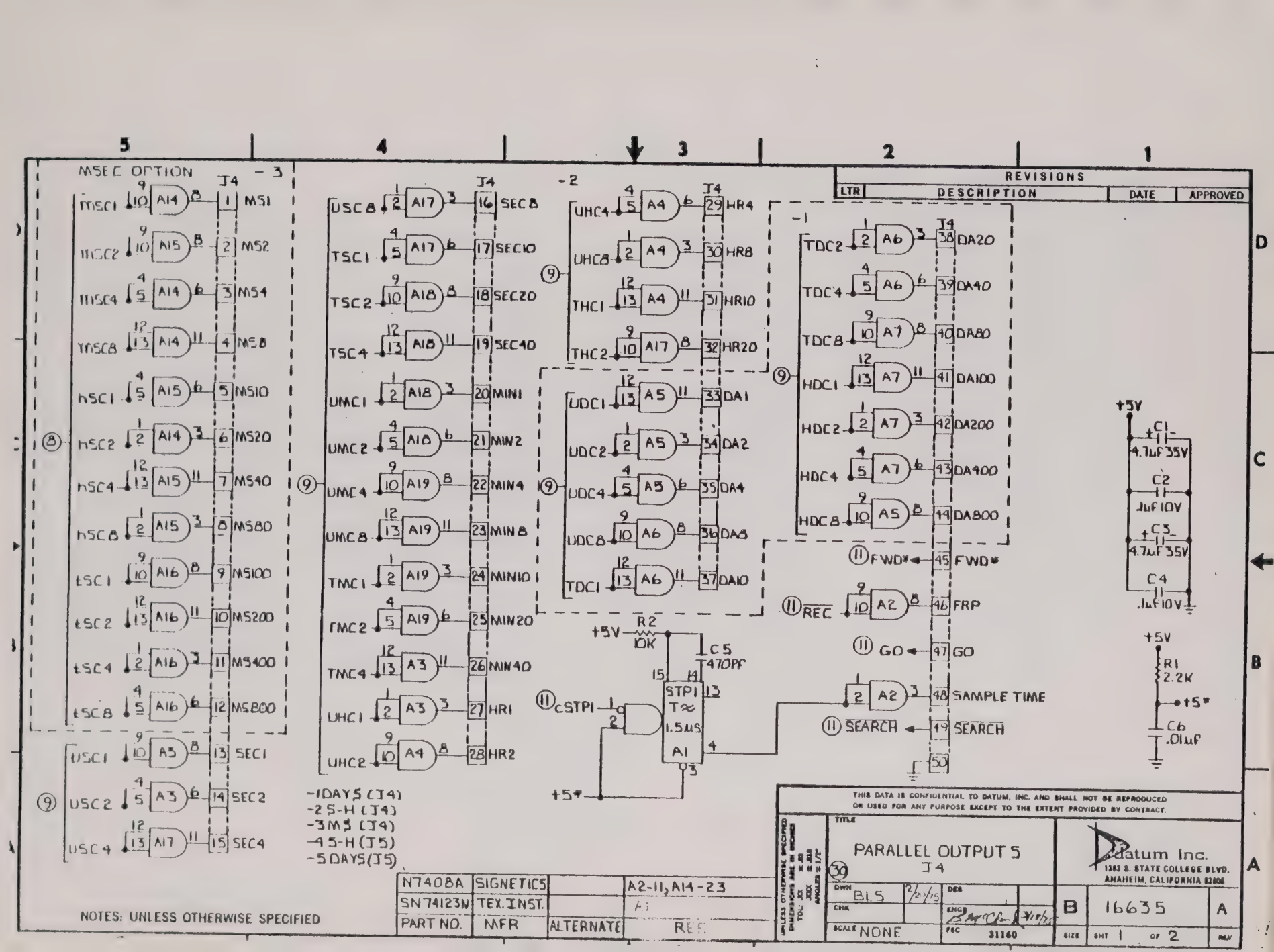
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03, XXX ±.010, ANGLES ±1/2°

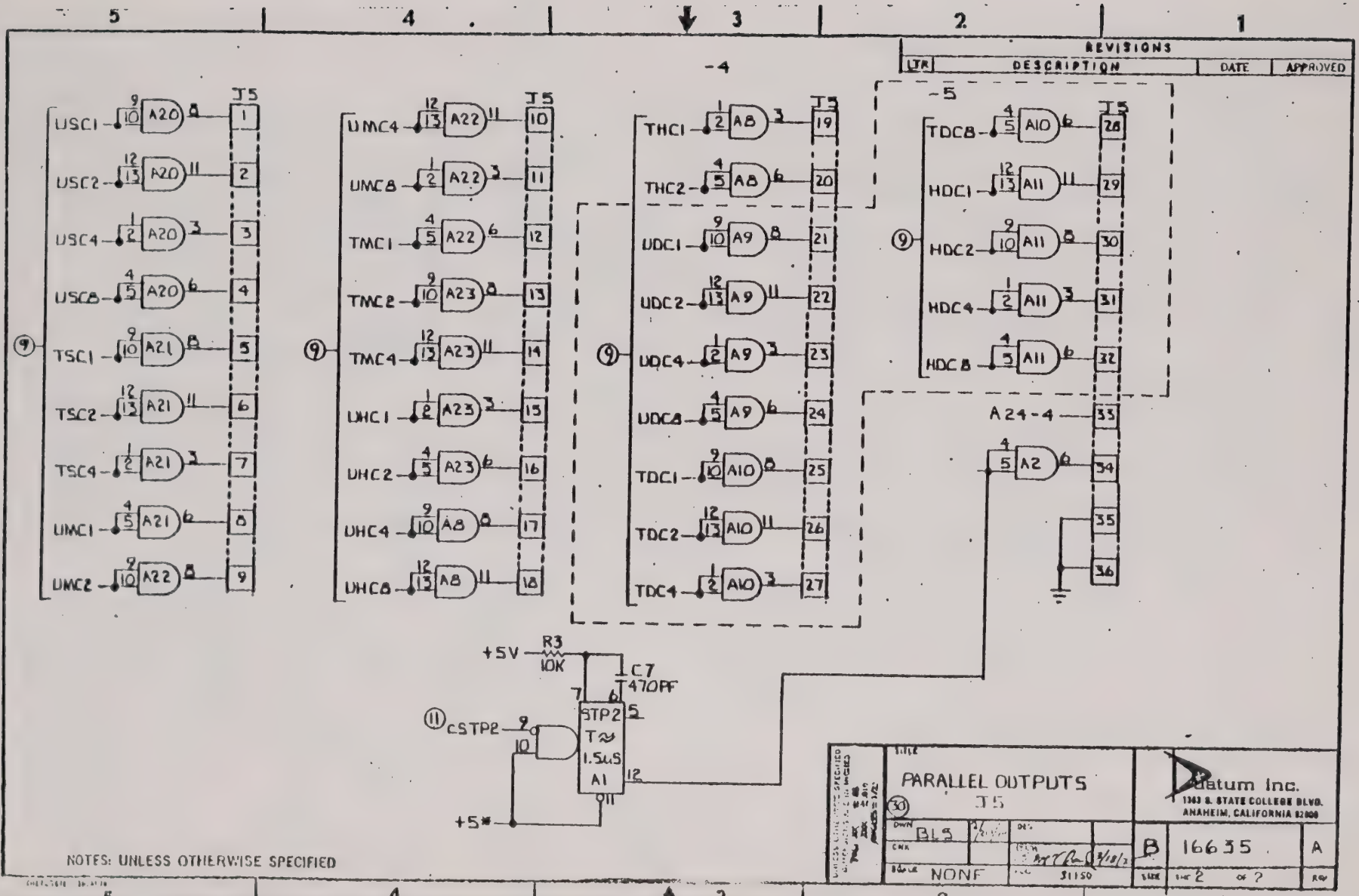
TITLE: LED DISPLAY (12)

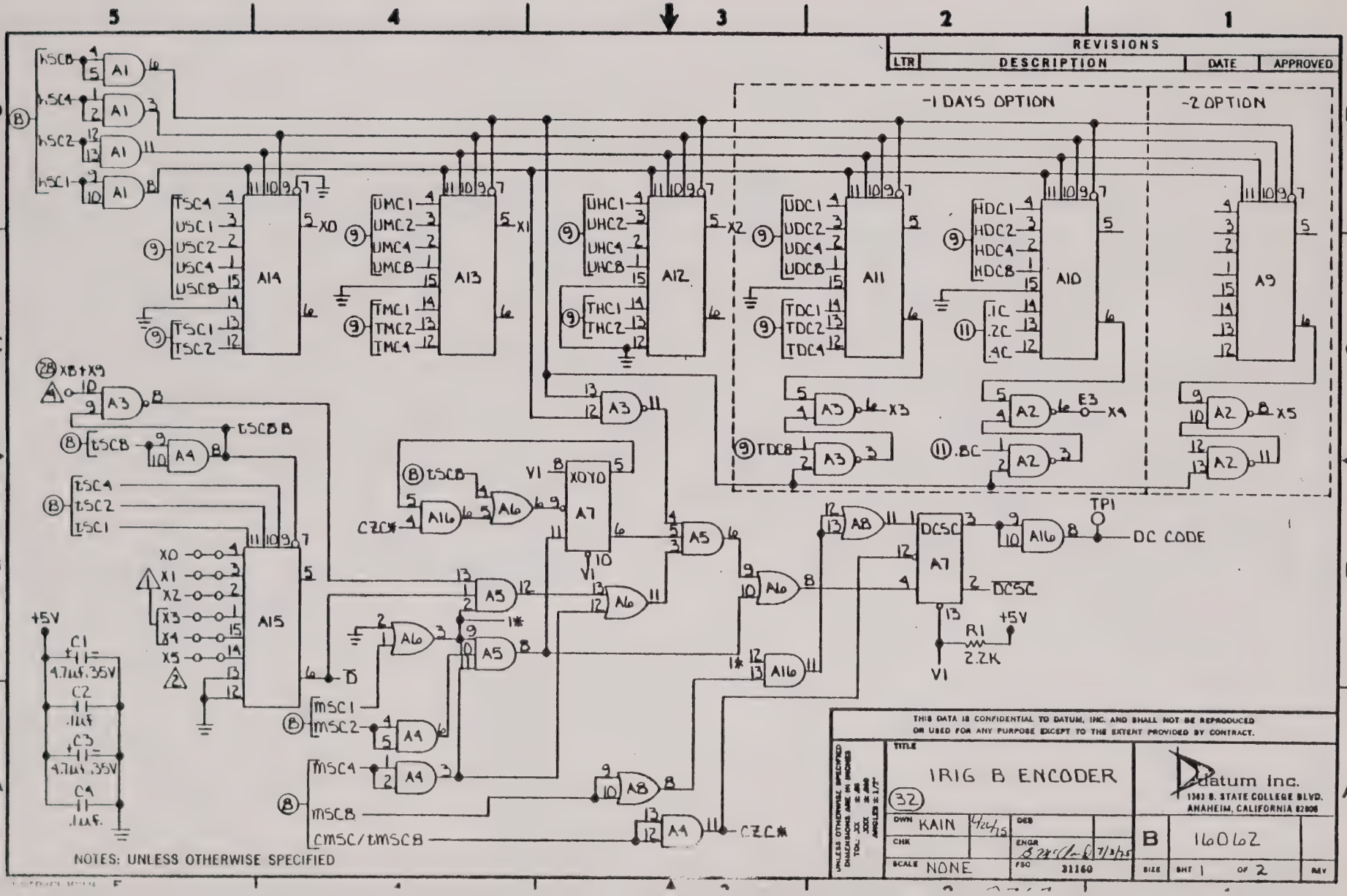
DWN IC 6/24/74 | DES | CHK | ENGR 11/4/74 | SCALE NONE | FSC 31160

Datum Inc.
1343 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

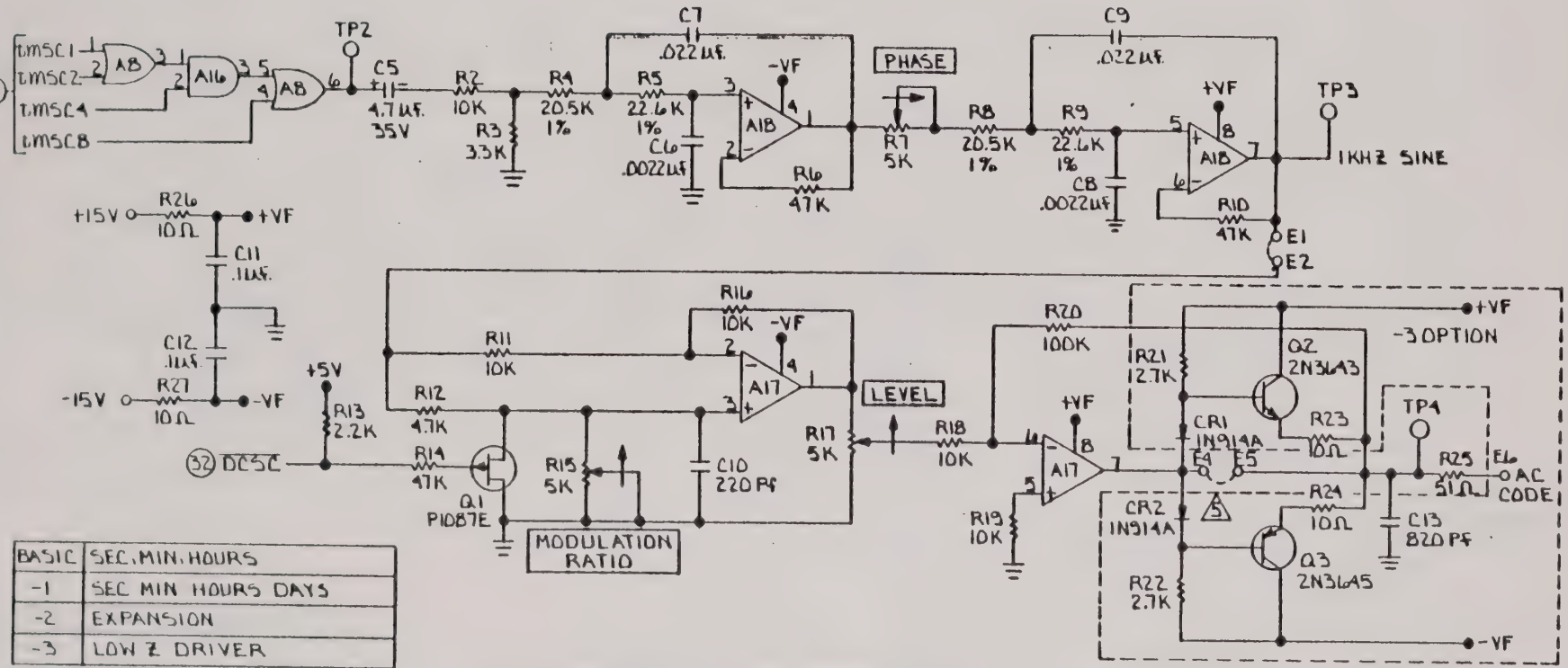
B | 16549 | SIZE | SHT 1 OF 1 | REV


MSEC OPTION -3
-2
-1
J4
MSI
MS2
MS4
MS8
MS10
MS20
MS40
MS80
MS100
MS200
MS400
MS800
SEC1
SEC2
SEC4
SEC8
SEC10
SEC20
SEC40
MIN1
MIN2
MIN4
MIN8
MIN10
MIN20
MIN40
HR1
HR2
HR4
HR8
HR10
HR20
DA1
DA2
DA4
DA8
DA10
DA20
DA40
DA80
DA100
DA200
DA400
DA800
FWD*
FRP
GO
SAMPLE TIME
SEARCH
-1DAY$ (J4)
-2 S-H (J4)
-3M$ (J4)
-4 S-H (J5)
-5DAYS(J5)
+5V
R2
10K
C5
470PF
STPI
T≈
1.5µs
cSTPI
+5*
C1
4.7µF 35V
C2
1µF 10V
C3
4.7µF 35V
C4
.1µF 10V
R1
2.2K
C6
.01µF
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
TITLE
PARALLEL OUTPUTS
J4
DWN BLS
CHK
ENGR
SCALE NONE
FSC 31160
Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
B
16635
A
SIZE
SHT 1 OF 2
REV
N7408A | SIGNETICS | | A2-11, A14-23
SN74123N | TEX. INST. | | A3
PART NO. | MFR | ALTERNATE | REF.
NOTES: UNLESS OTHERWISE SPECIFIED


REVISIONS
LTR DESCRIPTION DATE APPROVED
-4
-5
J5
USC1
USC2
USC4
USC8
TSC1
TSC2
TSC4
UMC1
UMC2
UMC4
UMC8
TMC1
TMC2
TMC4
UHC1
UHC2
UHC4
UHC8
THC1
THC2
UDC1
UDC2
UDC4
UDC8
TDC1
TDC2
TDC4
TDC8
HDC1
HDC2
HDC4
HDC8
A24-4
+5V
R3
10K
C7
470PF
STP2
T≈
1.5uS
A1
CSTP2
+5*
PARALLEL OUTPUTS
J5
Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
BLS
NONE
31150
B
16635
A
SHT 2 OF 2
NOTES: UNLESS OTHERWISE SPECIFIED


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
-1 DAYS OPTION
-2 OPTION
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
XO
X1
X2
X3
X4
X5
TP1
DC CODE
DCSC
R1
2.2K
+5V
C1
4.7uf. 35V
C2
.1uf
C3
4.7uf. 35V
C4
.1uf.
CZC*
V1
NOTES: UNLESS OTHERWISE SPECIFIED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
TITLE
IRIG B ENCODER
(32)
DWN KAIN 4/24/75
CHK
SCALE NONE
ENGR 7/3/75
FSC 31160
Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
B
160162
SIZE
SHT 1 OF 2
REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



BASIC	SEC, MIN, HOURS
-1	SEC MIN HOURS DAYS
-2	EXPANSION
-3	LOW Z DRIVER

N5558V	SIGNETICS	A17, A18
N74151N	T.I.	A9-15
N74107A	NATIONAL	A7
N7432A	↕	A6, 8
N7411A	↕	A5
N7408A	↕	A1, A4, A16
N7400A	NATIONAL	A2, A3
PART NO.	MFR	

5 REMOVE JUMPER FROM E4-E5 WHEN -3 OPTION IS USED.

4 GROUND WHEN 17 BIT BINARY NOT USED.

3 GROUND PIN14 WHEN -2 OPTION IS NOT USED.

1 CUT ETCH AND GROUND PINS 1 & 15 WHEN DAYS OPTION IS NOT USED.

NOTES: UNLESS OTHERWISE SPECIFIED

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: IRIG B ENCODER (32A)

DWN KAIN 6/24/75 DES

CHK ENGR 7/3/75

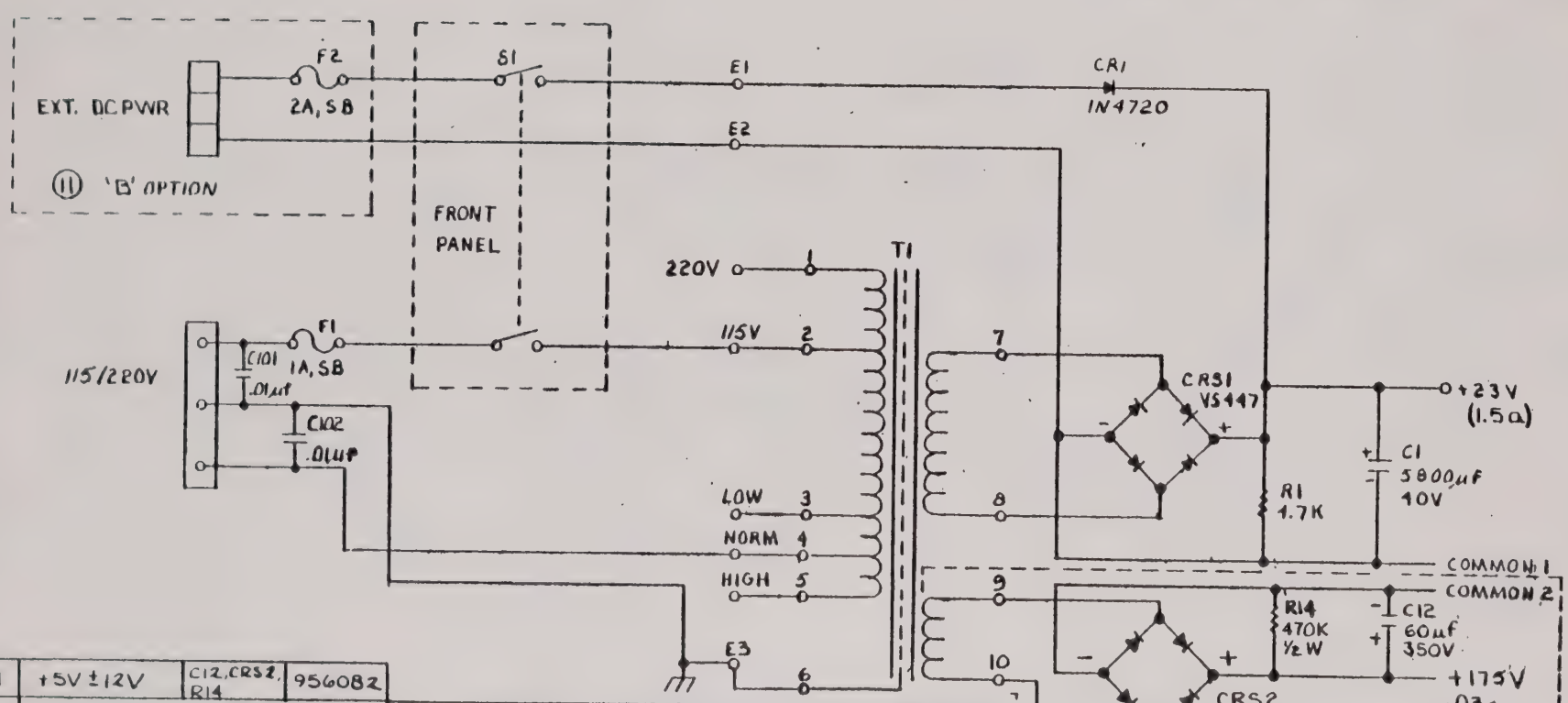
SCALE NONE FSC 31160

Datum Inc. 1363 S. STATE COLLEGE BLVD. ANAHEIM, CALIFORNIA 92806

B 16062

SIZE SHT 2 OF 2 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	C4 WAS 948901 SELECTED 47μF	6-26-73	RM



-11	+5V ±12V	C12, CRS2, R14	956082
A	INCLUDES ASSY 16742		
-10	+5V, ±8V	C12, CRS2, R14	956082
-9	-1, -3, -5, OR -7 USED WITH 16742		
-8	+5V, +12, -15, +175	C12	956088
DASH NO.		COMP. NOT USED	XFORMER USED
NOTES: UNLESS OTHERWISE SPECIFIED			

-7	+5V ± 15V	C12, CRS2, R14	956116
-6	+5V ± 15V +175V	C12	956088
-5	+5V, 12V, -15V	SEE NOTE 5.	956082
-4	+5V, ±15V, +175V		956088
-3	+5V, ±15V	C12, CRS2, R14	956082
-2	+5V, +175V	A2, A3, C8, C9, C10, C11, CR7, CR8	956088
-1	+5 ONLY	A2, A3, C8, C9, C10, C11, C12, CR7, CRS2, R14, CR8	956082
DASH NO.		COMP'S NOT USED	XFORMER USED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOL: .XX ±.03, .XXX ±.010, ANGLES ±1/2°

TITLE: POWER SUPPLY

(49)

DWN EK 3/13/73 DES RM 3/30

CHK

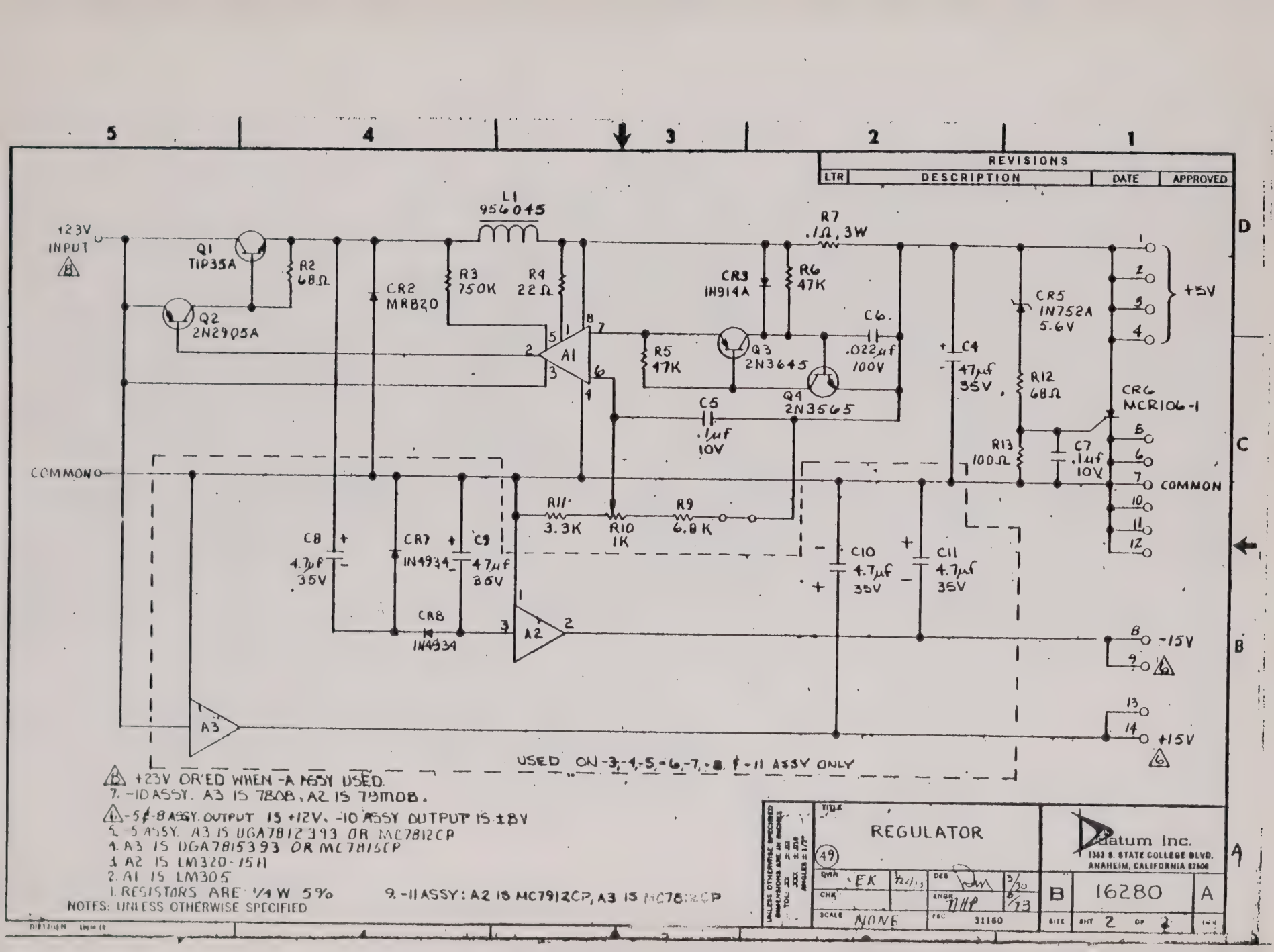
ENGR DMP 6/73

SCALE NONE PSC 31160

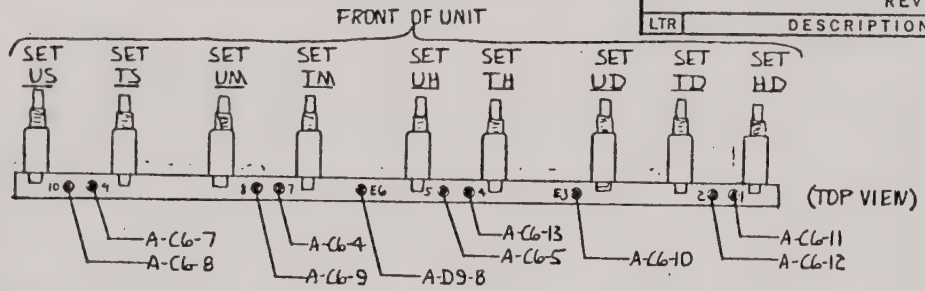
Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

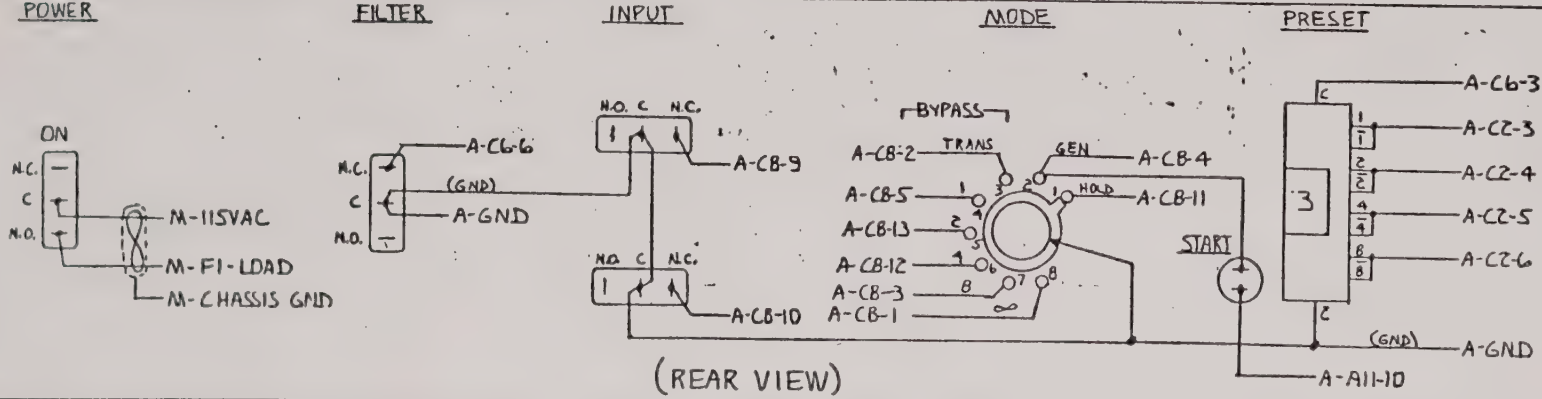
B | 16280 | A

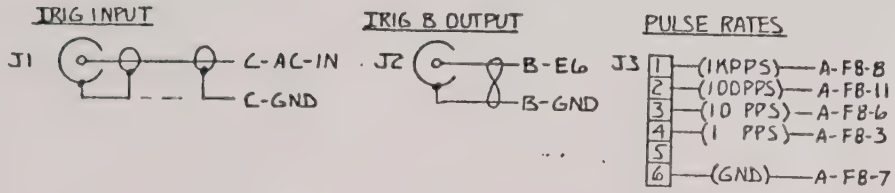
SIZE | SHT 1 OF 2


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
+23V INPUT
Q1 TIP35A
Q2 2N2905A
R2 68Ω
CR2 MRB20
L1 956045
R3 750K
R4 22Ω
A1
R5 47K
Q3 2N3645
Q4 2N3565
CR3 IN914A
R6 47K
R7 .1Ω, 3W
C6 .022µf 100V
C4 47µf 35V
C5 .1µf 10V
CR5 IN752A 5.6V
R12 68Ω
CR6 MCR106-1
R13 100Ω
C7 .1µf 10V
+5V
COMMON
R11 3.3K
R10 1K
R9 6.8K
C8 4.7µf 35V
CR7 IN4934
C9 47µf 35V
CR8 IN4934
A2
C10 4.7µf 35V
C11 4.7µf 35V
-15V
+15V
A3
USED ON -3, -4, -5, -6, -7, -8, & -11 ASSY ONLY
+23V OR'ED WHEN -A ASSY USED.
7. -10 ASSY. A3 IS 7808, A2 IS 79M08.
-5 & -8 ASSY. OUTPUT IS +12V, -10 ASSY OUTPUT IS ±8V
5. -5 ASSY. A3 IS UGA7812393 OR MC7812CP
4. A3 IS UGA7815393 OR MC7815CP
3. A2 IS LM320-15H
2. A1 IS LM305
1. RESISTORS ARE 1/4 W 5%
9. -11 ASSY: A2 IS MC7912CP, A3 IS MC7812CP
NOTES: UNLESS OTHERWISE SPECIFIED
TITLE
REGULATOR
(49)
DWN EK
CHK
SCALE NONE
DES
ENGR
FSC 31180
datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
B
16280
A
SIZE
SHT 2 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED







NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: 9300 – BASIC FRONT & REAR PANEL WIRING

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	DES		
CHK		ENGR	11/15/
SCALE		FSC 31160	

B 803485

SIZE SHT OF REV

SECTION VIII
LIST OF MATERIALS

1.	Time Code Generator/Translator	9300-708
2.	Time Code Generator/Translator	9300-001
3.	AGC	16085
4.	IRIG Basic	16543-136
5.	LED Display	16549-1
6.	Parallel Outputs	16635-123
7.	IRIG B Encoder	16062-1
8.	Power Supply	16280-3

DATE: 1-6-75
DRAWN: R. FLOCK
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:
REV

TITLE: TIME CODE GENERATOR/TRANSLATOR

ASS'Y NO: 9300-708

SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	9300-001	BASIC ASSY STK	DATUM	1			
2	SK9300-708	SHIPPING KIT	"	1			
4	703335-1	BUTCH PLATE STK	"	1			
6	16543-136	BASIC	"	1	(1)		
7	16635-123	PARALLEL OUTPUTS	"	1			

NOTES: (1) MODIFY 16543-16 IN BASIC UNIT (9300-001)

DATE: 10-25-74
DRAWN: BLS
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:
REV: A

TITLE: TIME CODE GEN/TRANS

ASS'Y NO: 9300-001

SHT 1 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	1202-0102	SWITCH SPDT	DATUM	4			
2	1204-3903	" P/B	"	10			
3	1206-5112-N	" SPI-12 POS	"	1			
4	1212-7606	" T/W	"	1			
5	1299-765G-1	BAND HARDWARE	"	1			
6	1704-1002	CONNECTOR BNC.	"	2			
7	" -1625-6R	" 6P	"	1			
8	1792-1855	CONTACT SOCKET	"	6			
9	1795-0001	WASHER	"	2			
10	" -0002	"	"	2			
11	2524-5010	KNOB	"	1			
12							
13	700362	CTR SUPPORT STK	"	1			
14	700364-2	COVER STK	"	2			
15	700425	MTG BRKT STK	"	2			
16	700546	STIFFENER STK	"	3			
17	704757-2	SIDE GUSSET STK	"	2			
18							
19	704899	REAR PANEL STK	"	1			
20	705853	COVER PLATE STK	"	1			
21	705850	FRONT PANEL STK	"	1			
22	705866-3	LENS STK	"	1			
23							
24	931500	HANDLE STK	"	2			
25							
26	170979	PC BOARD STK	"	1			

NOTES:

DATE: 10-25-74
DRAWN: BLS
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

REV A

TITLE: TIME CODE GEN/TRANS

ASS'Y NO: 9300-001

SHT 2 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
27	16062-1	IRIG ENCODER	DATUM	1			
28	16085	AGC STK	"	1			
29	16280-3	POWER SUPPLY STK	"	1			
30	16543-16	BASIC	"	1			
31	16549-1	DISPLAY	"	1			

NOTES:

DATE: 3-6-75
DRAWN: GKE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

G

TITLE: A G C

ASS'Y NO: 16085

SHT / OF

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	0102-0330	RESISTOR 33Ω ¼W 5%	DATUM	1	R10		
2	" -0910	" 91Ω " "	"	1	R3		
3	" -0391	" 390Ω " "	"	1	R44		
4	" -0511	" 510Ω " "	"	1	R18		
5	" -0561	" 560Ω " "	"	1	R17		
6	" -0102	" 1K " "	"	7	R21,22,26,33,38,43,45		
7	" -0122	" 1.2K " "	"	1	R37		
8	" -0152	" 1.5K " "	"	1	R30		
9	" -0202	" 2K " "	"	1	R46		
10	" -0272	" 2.7K " "	"	3	R25,32,39		
11	" -0302	" 3K " "	"	1	R31		
12	" -0512	" 5.1K " "	"	8	R4,8,12-14,20,34,40		
13	" -0682	" 6.8K " "	"	1	R29		
14	" -0752	" 7.5K " "	"	1	R16		
15	" -0103	" 10K " "	"	7	R5-7,11,28,36,41		
16	" -0183	" 18K " "	"	1	R24		
17	" -0473	" 47K " "	"	1	R23		
18	" -0753	" 75K " "	"	1	R19		
19	" -0124	" 120K " "	"	4	R2,9,15,35		
20	" -0274	" 270K " "	"	1	R47		
21	" -0105	" 1M " "	"	3	R1,27,42		
22	0104-0221	" 220Ω ½W "	"	1	R48		
23							
24	0220474	CAPACITOR .47μf 35V	"	2	C4,8		
25	" -0105	" 1μf "	"	6	C2,15,16,19-21		
26	" -0475	" 4.7μf "	"	5	C3,12,13,17,18		

NOTES:

DATE: 3-6-75
DRAWN: GHP
CHK:

MATERIAL LIST

Datum inc.

JOB NO:
QUANTITY:
REV G
TITLE: AGC
ASS'Y NO: 16085
SHT 2 OF 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
27	0220-0107	CAPACITOR 100Mf 10V	DATUM	1	C14		
28	0221-0221	" 220Mf 4V	"	2	C11A, 11B		
29	0225-0471	" 470Pf	"	1	C22		
30	" -0152	" 1500Pf	"	1	C10		
31	0226-0100	" 10Pf	"	1	C6		
32	" -0470	" 47Pf	"	1	C9		
33	" -0103-1	" .01Mf 100V	"	1	C7		
34	" -0203	" .02Mf "	"	1	C5		
35	" -0104-1	" .1Mf "	"	1	C1		
36							
37	0301-7405	FC N7405A	"	1	A5		
38	" -7749	" X6A7749393	"	2	A1,4		
39	" -9311-H	" LM311H	"	2	A2,3		
40							
41	0500-0306	DIODE 1N914A	"	2	CR1,3		
42	0515-0105-1	" 1N705A	"	1	CR2		
43	" -0752-1	" 1N752A	"	1	CR4		
44							
45	0550-7705	TRANSISTOR 2N3565	"	1	Q6		
46	0555-6600	" 2N3645	"	1	Q7		
47	0570-1057	" P1087E	"	3	Q3-5		
48	" -8703	" U1487E	"	1	Q2		
49	" -8704	" 988704	"	1	Q1		
50							
51							
52							

NOTES:

DATE: 3-6-75
DRAWN: GHE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

G

TITLE: AGC

ASS'Y NO: 16085

SHT 3 OF

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
53	1708-3100-1	SOCKET 14P	DATUM	3			
54	" -8000	" 8P	"	2			
55							
56	170574E	PC BOARD STK	"	1			
57	170785NC	" STK	"	1			

NOTES:

DATE: 10-16-74
DRAWN: RAE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:
REV: C

TITLE: IRIG BASIC

ASS'Y NO: 16543-136

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	0102-0151	RESISTOR 150Ω 1/4W 5%	DATUM	1	R3		
2	" -0102	" 1K " "	"	1	R4		
3							
4	" -0512	" 5.1K " "	"	1	R1		
5	" -0562	" 5.6K " "	"	3	R9-11		
6	" -0103	" 10K " "	"	1	R2		
7							
8	0126-R6K0	" CHIP 6K	"	2	C6,8		
9							
10	0220-0475	CAPACITOR 4.7MF 35V	"	7	C3,14-17,22,23		
11	0225-0330	" 33PF	"	3	C10-12		
12	" -0221	" 220PF	"	2	C1,2		
13	" -0331	" 330PF	"	2	C9,13		
14	0221-0685	" 6.8μf 35V	"	1	C25		
15	0226-0104	" .1MF 10V	"	5	C18-21,24		
16							
17							
18							
19	0301-7H03	IC SN74H103N	"	1	F10		
20	" -7H06	" SN74H106N	"	1	+ D4		
21	" -7123	" SN74123N	"	2	+ B11, D5		
22	" -7156	" SN74156N	"	2	+ C5,7		
23	" -7157	" SN74157N	"	3	+ C4, D7, E7		
24	" -7192	" SN74192N	"	10	+ B2-10, E4		
25	" -7194	" SN74194N	"	1	+ C2		
26	" -7400	" N7400A	"	3	A11, D2, 10		

NOTES:

DATE: 10-16-74
DRAWN: GAE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:
REV C

TITLE: IRIG BASIC

ASS'Y NO: 16543-136

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
27	0301-7404	IC N7404A	DATUM	1	D3		
28	" -7408	" N7408A	"	3	D9, F8, 9		
29	" -7410	" N7410A	"	1	D11		
30	" -7411	" N7411A	"	1	C9		
31	" -7425	" SN7425N	"	1	E8		
32	" -7432	" SN7432N	"	1	D6		
33	" -7442	" N7442B	"	1	* E6		
34	" -7473	" N7473A	"	1	E10		
35	" -7474	" SN7474N	"	2	E9, F11		
36	" -7486	" N7486A	"	2	C3, D8		
37	" -8280	" N8280A	"	5	E5, F4-7		
38	" -8281	" N8281A	"	2	C10, E11		
39	" -7122	" SN74122	"	1	C11		
40	" -9374	" 9374DC	"	9	* AZ-10		
41							
42							
43							
44	1301-0001	OSCILLATOR 1MHz	"	1	X1		
45							
46	1708-3897	SOCKET 14P W/W	"	27			
47	" -3898	" 16P "	"	29	*		
48							
49	2310-1591-B	MTG BLOCK	"	2			
50							
51	170969	PC BOARD	"	1			

NOTES:

DATE: 7-26-76
DRAWN: R. FLOCIC
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:
REV

TITLE: LED DISPLAY

ASS'Y NO: 16549-1

SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.				REF. DES.	UNIT COST	LOT TOTAL	
1	1708-0036	HEADER	DATUM	2							
3	" -3788	SOCKET	"	9							
5	2205-0006	LED DISPLAY	"	9				DS1-9			
7	170937	P.C. BD. STK	"	1							

NOTES:

DATE: 2-9-76
DRAWN: BLS
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

REV A

TITLE: PARALLEL OUTPUT

ASS'Y NO: 16635-123

SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.				REF. DES.	UNIT COST	LOT TOTAL	
1	0102-0222	RESISTOR 2.2K ¼W 5%	DATUM	1				R1			
2	" -0103	" 10K " "	"	1				R2			
3											
4	0220-0475	CAPACITOR 4.7μf 35V	"	2				C1, 3			
5	0225-0471	" 470 Pf	"	1				C5			
6	0226-0103-1	" .01μf 100V	"	1				C6			
7	" -0104	" .1μf 10V	"	2				C2, 4			
8											
9	0301-7123	IC SN74123N	"	1			*	A1			
10	" -7408	N7408A	"	12				A2-7, 14-19			
11											
12	1704-0050	CONNECTOR 50P	"	1				J4			
13											
14											
15	1708-3897	SOCKET 14P w/w	"	12							
16	" -3898	" 16P "	"	1			*				
17											
18	703336	CONN PLATE STK	"	1							
19											
20	171112	PC BOARD STK	"	1							

NOTES:

DE4

DATE: 10-20-75
DRAWN: RAE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:
REV

TITLE: IRIG ENCODER

ASS'Y NO: 16062-1

SHT 1 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	0102-0100	RESISTOR 10Ω 1/4W 5%	DATUM	2	R26,27		
2	" -0510	" 51Ω " "	"	1	R25		
3	" -0222	" 2.2K " "	"	2	R1,13		
4							
5	" -0332	" 3.3K " "	"	1	R3		
6	" -0472	" 4.7K " "	"	1	R12		
7	" -0103	" 10K " "	"	5	R2,11,16,18,19		
8	" -0473	" 47K " "	"	3	R6,10,14		
9	" -0104	" 100K " "	"	1	R20		
10	0115-2052	" 20.5K " 1%	"	2	R4,8		
11	" -2262	" 22.6K " "	"	2	R5,9		
12	0154-5001	" POT 5K	"	3	R7,15,17		
13							
14	0201-0221	CAPACITOR 220pf	"	1	C10		
15	0212-0222	" .0022μf 100V	"	2	C6,8		
16	" -0223	" .022μf "	"	2	C7,9		
17	0220-0475	" 4.7μf 35V	"	3	C1,3,5		
18							
19	0226-0104	" .1μf 10V	"	2	C2,4		
20	" -0104-1	" .1μf 100V	"	2	C11,12		
21							
22	0301-5558	IC N5558V	"	2	A17,18		
23	" -7107	" SN74107N	"	1	A7		
24	" -7151	" SN7415IN	"	6	* A10-15		
25	" -7400	" N7400A	"	2	A2,3		
26	" -7408	" N7408A	"	3	A1,4,16		

NOTES:

DATE: 10-20-75
DRAWN: QHE
CHK:

MATERIAL LIST

Datum inc.

JOB NO:
QUANTITY:
REV

TITLE: IRIG ENCODER
ASS'Y NO: 16062-1
SHT 2 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.				REF. DES.	UNIT COST	LOT TOTAL	
27	0301-7411	IC N7411A	DATUM	1				A5			
28	" -7432	" SN7432N	"	2				A6, 8			
29											
30											
31											
32											
33											
34	0570-1087	TRANSISTOR P1087E	"	1				Q1			
35											
36	1706-2010	TERMINAL	"	4				TP1-4			
37	1708-2034	SOCKET 8P	"	2							
38	" -3897	" 14P W/W	"	9							
39	" -3898	" 16P "	"	6			*				
40											
41	170518	PC BOARD STK	"	1							

NOTES:

DATE: 11-14-74
DRAWN: RAE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:
REV: A

TITLE: POWER SUPPLY +5V ±15V
ASS'Y NO: 16280-3
SHT 1 OF 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	0102-0220	RESISTOR 22Ω ¼W 5%	DATUM	1	R4		
2	" -0680	" 68Ω " "	"	2	R2,12		
3	" -0101	" 100Ω " "	"	1	R13		
4	" -0332	" 3.3K " "	"	1	R11		
5	" -0472	" 4.7K " "	"	1	R1		
6	" -0682	" 6.8K " "	"	1	R9		
7	" -0473	" 47K " "	"	2	R5,6		
8	" -0754	" 750K " "	"	1	R3		
9	0125-0R10	" .1Ω 3W	"	1	R7		
10	0151-1001	" POT 1K	"	1	R10		
11							
12	0212-0223	CAPACITOR .022μF 100V	"	1	C6		
13	0219-0588	" 5800μF 40V	"	1	C1		
14	0220-0475	" 4.7μF 35V	"	3	C8,10,11		
15	" -0476	" 47μF 35V	"	2	C9,4		
16							
17	0226-0103	" .01μF 1000V	"	2	C101,102		
18	" -0104	" .1μF 10V	"	2	C5,7		
19							
20	0301-7815	IC UGH7815393	"	1	A3		
21	" -9305	" LM305	"	1	A1		
22	" -9320	" LM320-15H	"	1	A2		
23							
24	0500-0306	DIODE 1N914A	"	1	CR3		
25	0515-0752-1	" 1N752A	"	1	CR5		
26	0540-0106-1	" MCR106-1	"	1	CR6		

NOTES:

DATE: 11-14-74
DRAWN: RHE
CHK:

MATERIAL LIST

Datum inc.

JOB NO:
QUANTITY:

REV: A

TITLE: POWER SUPPLY +5V,±15V

ASS'Y NO: 16280-3

SHT 2 OF 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
27	0540-0447	BRIDGE RECT VS447	DATUM	1	CR51		
28	" -0820	DIODE MR820	"	1	CR2		
29	" -4720-1	" IN4720	"	1	CR1		
30	" -4934	" IN4934	"	2	CR7,8		
31							
32	0550-035A	TRANSISTOR TIP-35A	"	1	Q1		
33	" -7705	" 2N3565	"	1	Q4		
34	0555-6005	" 2N2905A	"	1	Q2		
35	" -6600	" 2N3645	"	1	Q3		
36							
37	0601-6045	CHOKE	"	1	L1		
38	" -6082	TRANSFORMER	"	1	T1		
39							
40	0702-0010-1	FUSE 1A S/B 3AG	"	1	F1		
41							
42	0750-0200	" HOLDER	"	1	XF1		
43							
44	1704-1061-1	CONNECTOR AC	"	1			
45							
46	1706-0033	EYELET	"	2	(L1)		
47	1708-3897	SOCKET 14P W/W	"	1			
48	" -8000	" 8P	"	1	XA1		
49							
50							
51	2310-1247-09	STANDOFF	"	1	(L1)		
52	2325-1004	TOROID RETAINER	"	2	(L1)		

NOTES:

DATE: 11-14-74
DRAWN: GHE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

REV A

TITLE: POWER SUPPLY +5V, ±15V

ASS'Y NO: 16280-3

SHT 3 OF 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
53	704561	MTG PLATE STK	DATUM	1			
54	704562	SIDE BRKT STK	"	1			
55	704563	HEATSINK STK	"	1			
56	704966-1	MTG BRKT STK	"	1			
57	704966-2	" " STK	"	2			
58							
59	170778	PC BOARD STK	"	1			
60	170779	" " STK	"	1			

NOTES:

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